



MMC 4051 MMC 4052 MMC 4053

# ANALOG MULTIPLEXERS-DEMULTIPLEXERS:

- 4051 SINGLE 8-CHANNEL**
- 4052 DIFFERENTIAL 4-CHANNEL**
- 4053 TRIPLE 2-CHANNEL**
- GENERAL DESCRIPTION**

The MMC 4051, MMC 4052 and MMC 4053 are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic package. MMC 4051, MMC 4052 and MMC 4053 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD}-V_{SS}$  and  $V_{DD}-V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic „1“ is present at the inhibit input terminal all channel are off. The MMC 4051 is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The MMC 4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The MMC 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

## FEATURES

- Low „ON“ resistance: 125 ohm (typ.) over 15 Vp.p. signal-input range for  $V_{DD}-V_{EE} = 15$  V
- High „OFF“ resistance: channel leakage  $\pm 100$  pA (typ.)  $V_{DD}-V_{EE} = 18$  V
- Binary address decoding on chip
- Very low quiescent power dissipation under all digital control input and supply conditions: 0.2  $\mu$ W (typ.),  $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10$  V
- Matched switch characteristics:  $R_{ON} = 5$  ohm (typ.) for  $V_{DD}-V_{EE} = 15$  V
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 Vp.p.

## ABSOLUTE MAXIMUM RATINGS

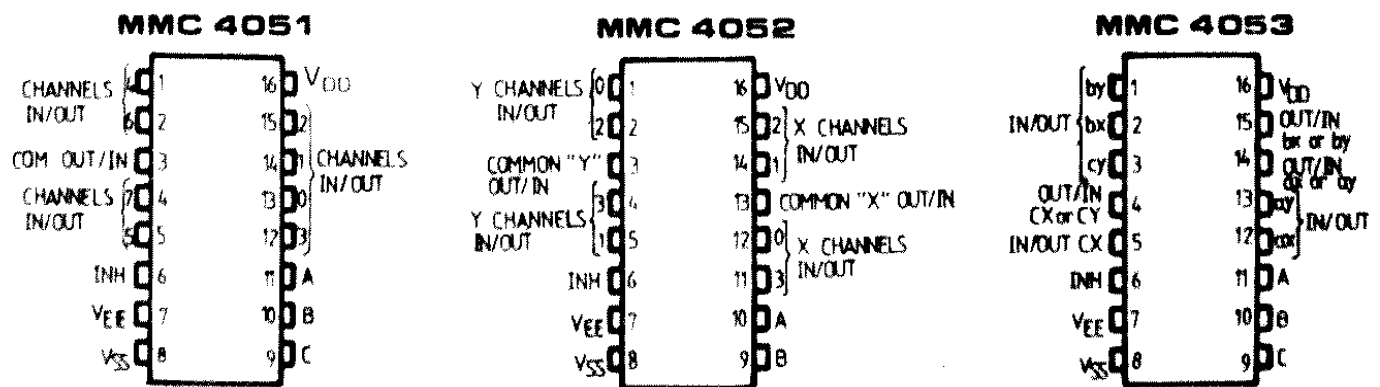
$V_{DD}^*$	Supply voltage: G and H types E and F types	-0.5 to	20	V
$V_i$	Input voltage	-0.5 to	18	V
$I_i$	DC input current (any one input)	-0.5 to	$V_{DD}+0.5$	V
$P_{tot}$	Total power dissipation (per package)		$\pm 10$	mA
	Dissipation per output transistor for $T_A =$ full package-temperature range		200	mW
$T_A$	Operating temperature: G and H types E and F types		100	mW
$T_{stg}$	Storage temperature	-55 to	125	°C
		-40 to	85	°C
		-65 to	150	°C

\* All voltage values are referred to  $V_{SS}$  pin voltage

## RECOMMENDED OPERATING CONDITIONS

$V_{DD}^*$	Supply voltage: G and H types E and F types	3 to	18	V
$V_i$	Input voltage	3 to	15	V
		0 to	$V_{DD}$	V
$T_A$	Operating temperature: G and H types E and F types	-55 to	125	°C
		-40 to	85	°C

## CONNECTION DIAGRAMS



**MMC 4051 MMC 4052 MMC 4053**

**STATIC ELECTRICAL CHARACTERISTICS**

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	T <sub>LOW</sub>		25°C			T <sub>HIGH</sub>			
						min.	max.	min.	typ.	max.	min.		max.	
I <sub>L</sub>	quiescent device current	G, H types				5		5	0.04	5		150	μA	
						10		10	0.04	10		300		
						15		20		0.04	20			600
						20		100		0.08	100			3000
	E, F types			5		20		0.04	20		150			
				10		40		0.04	40		300			
			15		80		0.04	80		600				

**Switch**

ON-resistance	G, H types	0 ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	0	0	5		880		470	1050		1200	Ω
					10		310		180	400		580	
					15		220		125	280		400	
	E, F types	0 ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	0	0	5		880		470	1050		1200	
					10		330		180	400		520	
					15		230		125	280		360	
ΔON-resistance (between any 2 channels)			0	0	5			10					Ω
OFF (●) leakage current	Any channel OFF	G, H types	0	0	18		100		±0.1	100		1000	nA
	All channels OFF (common OUT/IN)	G, H types	0	0	18		100		±0.1	100		1000	nA
	Any channel OFF	E, F types	0	0	15		300		±0.1	300		1000	nA
	All channels OFF (common OUT/IN)	E, F types	0	0	15		300		±0.1	300		1000	nA
C-capacitance	Input							5					pF
	Output 4051		-5	-5	5			30					
	Output 4052							18					
	Output 4053							9					
Feedthrough								0.2					

**Control (Address or Inhibit)**

V <sub>IL</sub>	Input low voltage	= V <sub>DD</sub> thru 1KΩ	V <sub>EE</sub> = V <sub>SS</sub> R <sub>I</sub> = 1KΩ to V <sub>SS</sub>	5		1.5			1.5		1.5	V
				10		.3		3		3		
				15		4		4		4		
V <sub>IH</sub>	Input high voltage		I <sub>IS</sub> > 2μA (on all OFF channels)	5	3.5		3.5			3.5		V
				10	7		7		7			
				15	11		11		11			

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**STATIC ELECTRICAL CHARACTERISTICS**

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT	
		V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	T <sub>LOW</sub>		25°C			T <sub>HIGH</sub>		
						min.	max.	min.	typ.	max.	min.		max.
I <sub>IH</sub> , I <sub>IL</sub> Input leakage current	G, H types	V <sub>I</sub> = 0/18 V			18		±0.1		±10 <sup>-3</sup>	±0.1		±1	μA
	E, F types	V <sub>I</sub> = 0/15 V			15		±0.3		±10 <sup>-3</sup>	±0.3		±1	
C <sub>I</sub> Input capacitance		Any address or inhibit input							5	7.5			pF

(o) Determined by minimum feasible leakage measurement for automatic testing

(\*) T<sub>Low</sub> = -55°C for G, H device; -40°C for E, F device.


T<sub>High</sub> = +125°C for G, H device; +85°C for E, F device.

**DYNAMIC ELECTRICAL CHARACTERISTICS**

(T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, all input square wave rise and fall time = 20 ns)

PARAMETER	TEST CONDITIONS						VALUES		UNIT
	V <sub>EE</sub> (V)	R <sub>L</sub> (KΩ)	f <sub>i</sub> (KHz)	V <sub>IS</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	typ.	max.	

**Switch**

t <sub>pd</sub> Propagation delay time (Signal input to output)		200		10 V 		5 10 15			30 15 11	30 60 20	ns
Frequency response channel „ON“ (Sine wave Input) at 20 Log $\frac{V_0}{V_i} = -3$ dB	= V <sub>SS</sub>	1		5(*)		10	V <sub>O</sub> at common OUT/IN	4053 4052 4051	30 25 20		MHz
							V <sub>O</sub> at any channel		60		MHz
Feedthrough (all channels OFF) at 20 Log $\frac{V_0}{V_i} = -40$ dB	= V <sub>SS</sub>	1		5(*)		10	V <sub>O</sub> at common OUT/IN	4053 4052 4051	8 10 12		MHz
							V <sub>O</sub> at any channel		8		MHz
Frequency signal crosstalk at 20 Log $\frac{V_0}{V_i} = -40$ dB	= V <sub>SS</sub>	1		5(*)		10	Between any 2 channels		3		MHz
							Between sections 4052 only	Measured on common	6		
								Measured on any channel	10		
Between any 2 sections 4053 only	In pin 2 out pin 14	2.5									
	In pin 15 out pin 14	6									
Sine wave distortion: f <sub>IS</sub> = 1 KHz sine wave	= V <sub>SS</sub>	10 10 10	1 1 1	2(*) 3(*) 5(*)		5 10 15		0.3 0.2 0.12		%	

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PARAMETER	TEST CONDITIONS						VALUES		UNIT
	V <sub>EE</sub> (V)	R <sub>L</sub> (K)	f <sub>i</sub> (KHz)	V <sub>IS</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	typ.	max.	

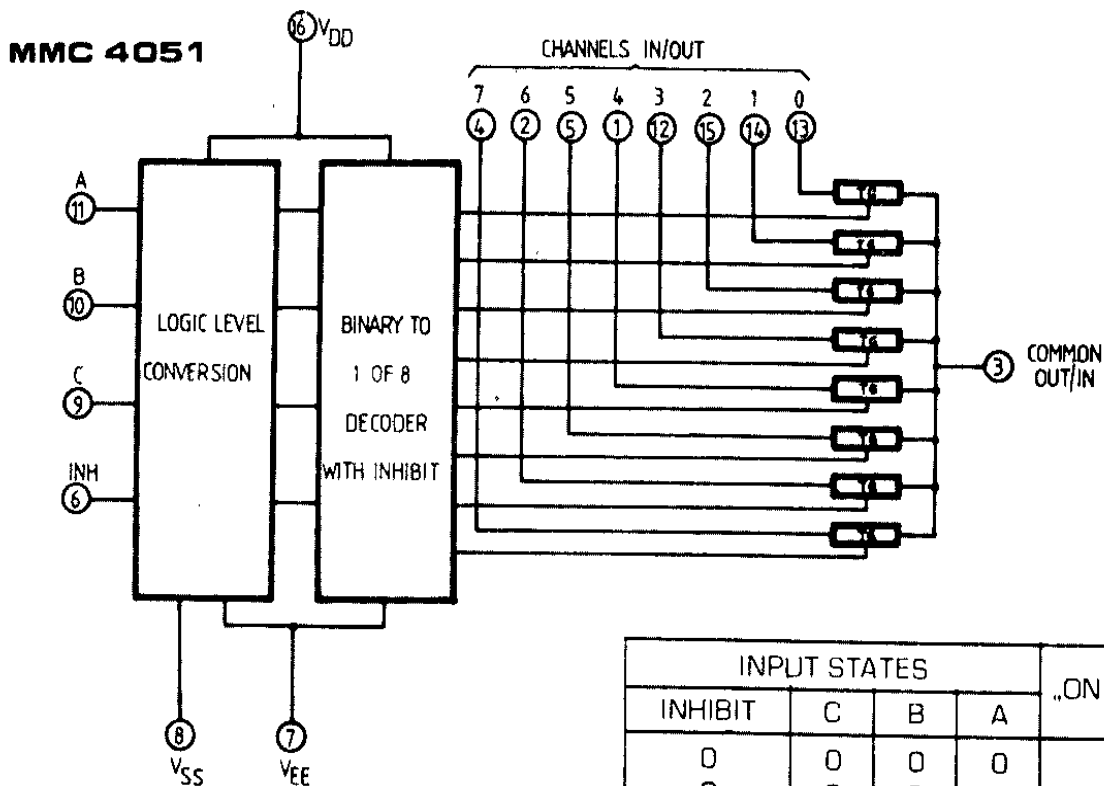
**Control (address or inhibit)**

Propagation delay time: Address-to signal OUT channels ON or OFF	0 0 0 - 5				0 0 0 0	5 10 15 5		360 160 120 225	720 320 240 450	ns
Propagation delay time: Inhibit to signal OUT (channel turning ON)	0 0 0 - 10	10			0 0 0 0	5 10 15 5		360 160 120 200	720 320 240 400	ns
Propagation delay time: Inhibit to signal OUT (channel turning OFF)	0 0 0 - 10	0.3				5 10 15 5		200 90 70 130	450 210 160 300	ns
Address or inhibit to signal crosstalk	0	10%			0	10	V <sub>C</sub> = V <sub>DD</sub> - V <sub>SS</sub> (Square wave)	65		mV peak

● Peak to peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$

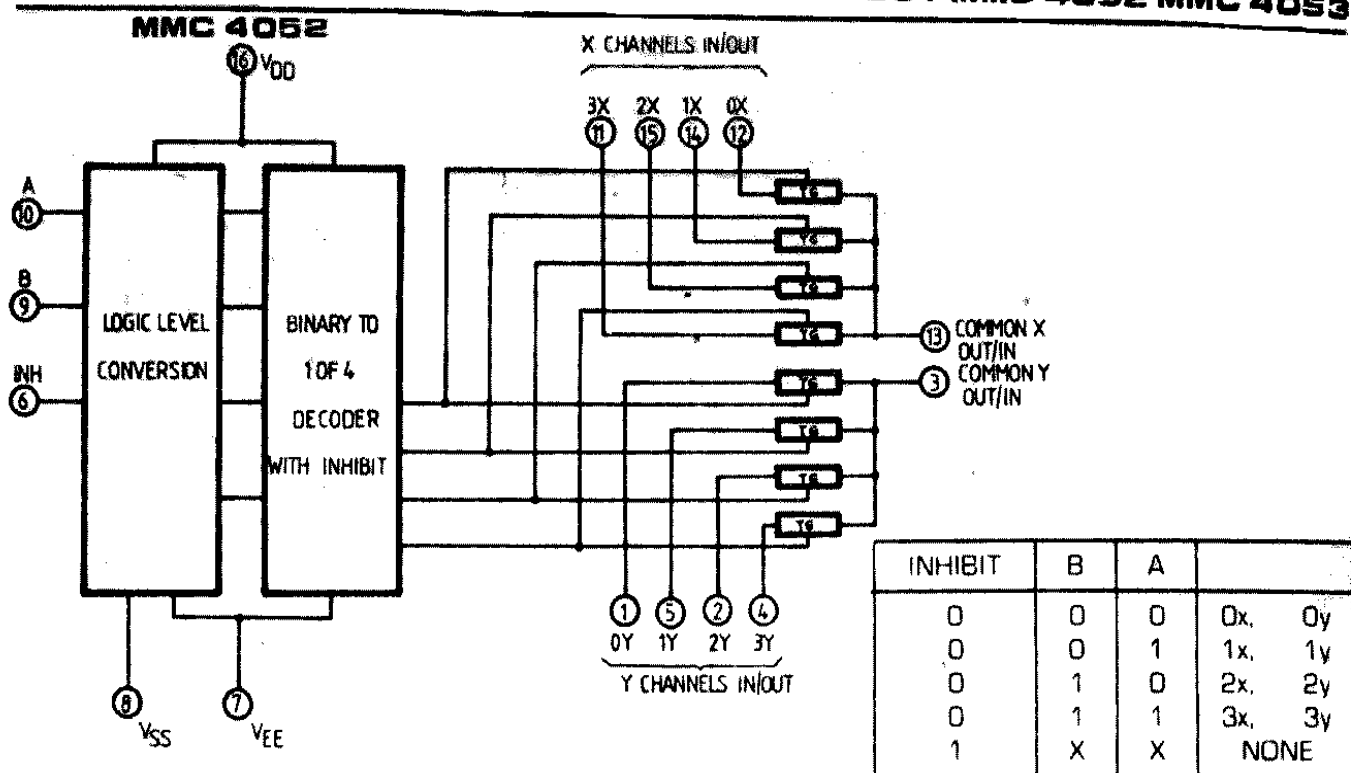
(%) Both ends of channel.

**FUNCTIONAL DIAGRAMS AND TRUTH TABLES**

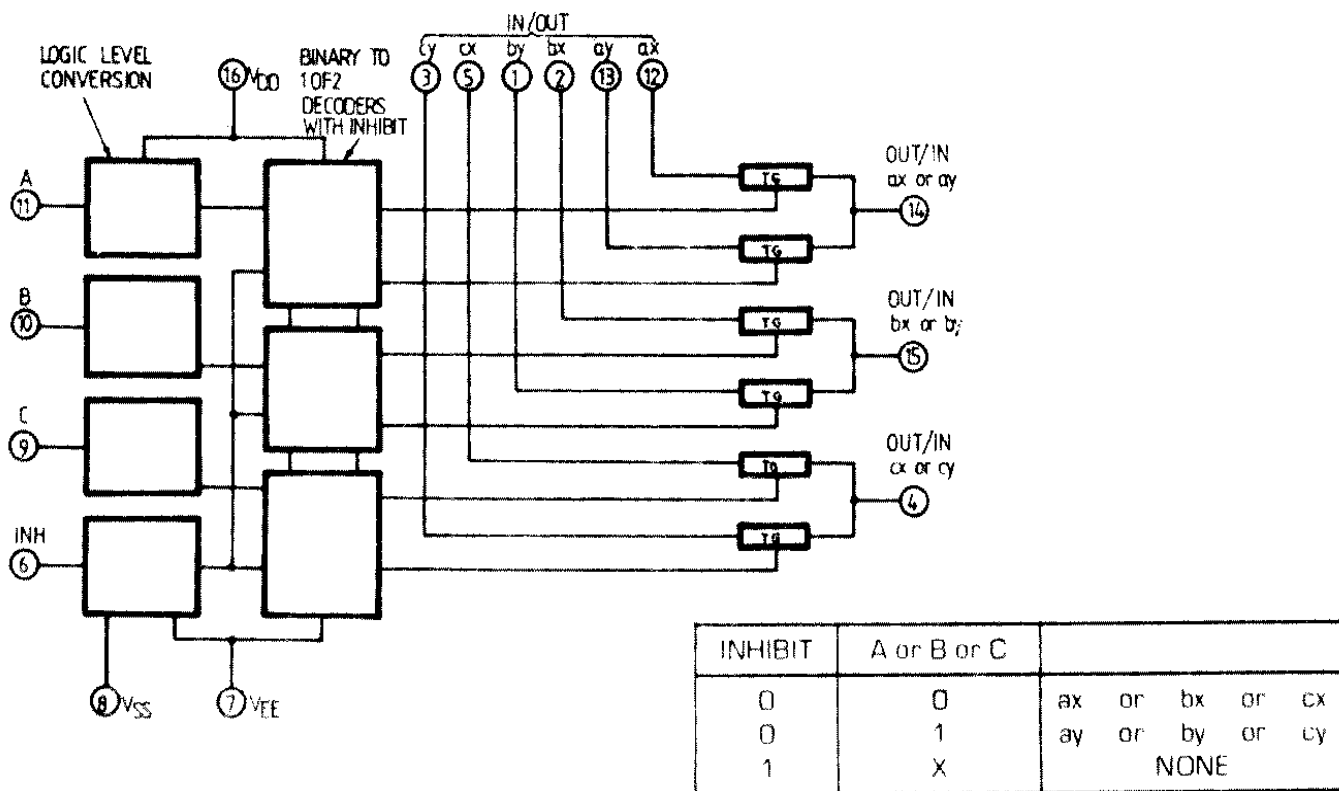


INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE

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**SPECIAL CONSIDERATIONS**

Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if  $V_{DD} - V_{SS} = 3\text{ V}$ , a  $V_{DD} - V_{EE}$  of up to 13 V can be controlled, for  $V_{DD} - V_{EE}$  level differences above 13 V, a  $V_{DD} - V_{SS}$  of at least 4.5V is required). For example, if  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = 0$ , and  $V_{EE} = -13.5\text{ V}$ , analog signals from  $-13.5\text{ V}$  to  $+4.5\text{ V}$  can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt. No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into lead 3 on the MMC 4051; leads 3 and 13 on the MMC 4052; leads 4, 14, 15 on the MMC 4053