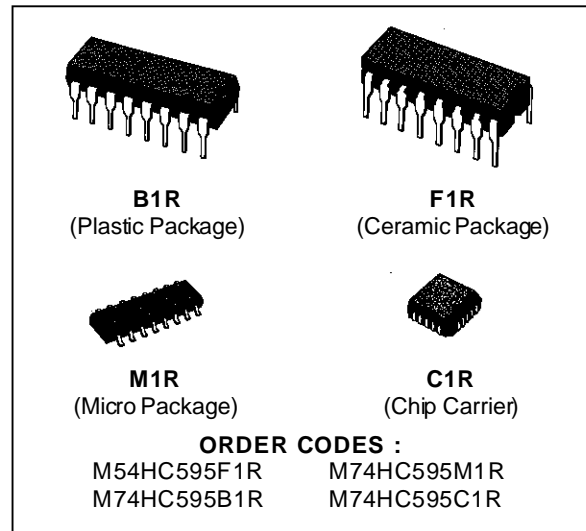


8 BIT SHIFT REGISTER WITH OUTPUT LATCHES (3 STATE)

- HIGH SPEED
 $f_{MAX} = 55 \text{ MHz (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 15 LSTTL LOADS FOR QA TO QH
 10 LSTTL LOADS FOR QH'
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.) FOR QA TO QH}$
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.) FOR QH'}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH LSTTL 54/74LS595



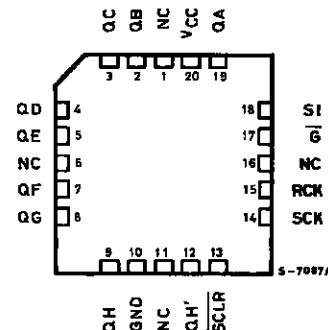
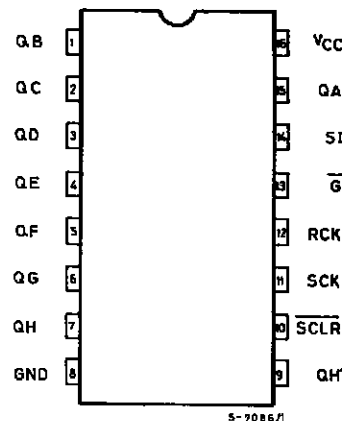
DESCRIPTION

The M54/74HC595 is a high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated in silicon C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.

The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT

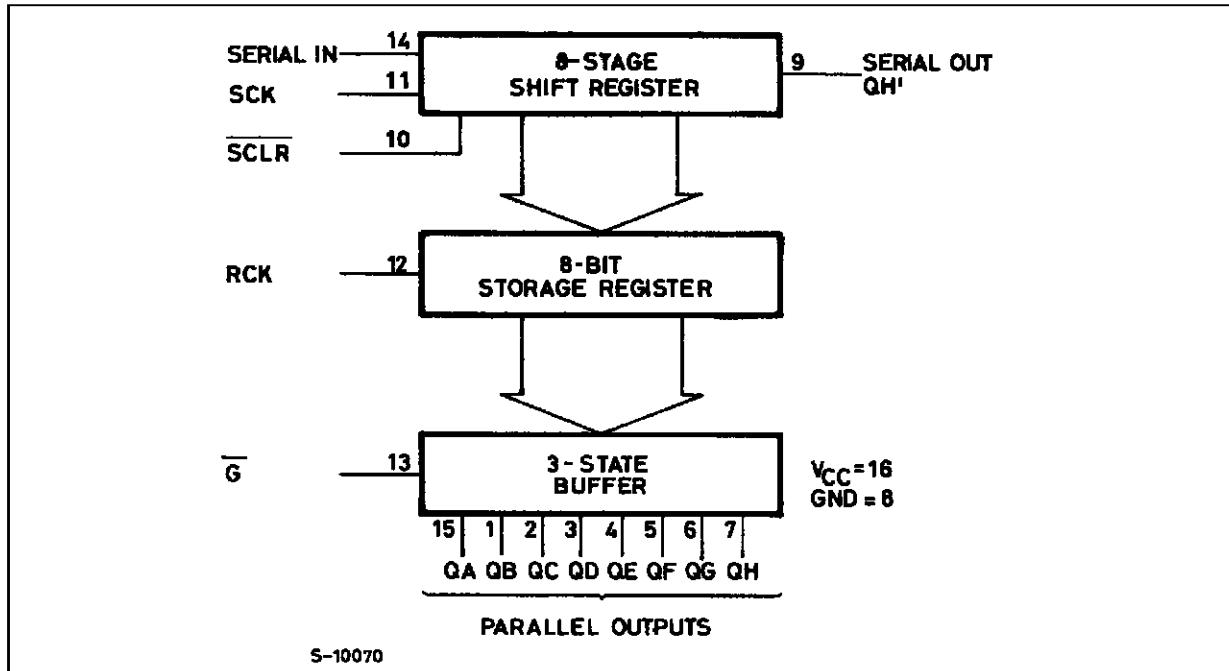


TRUTH TABLE

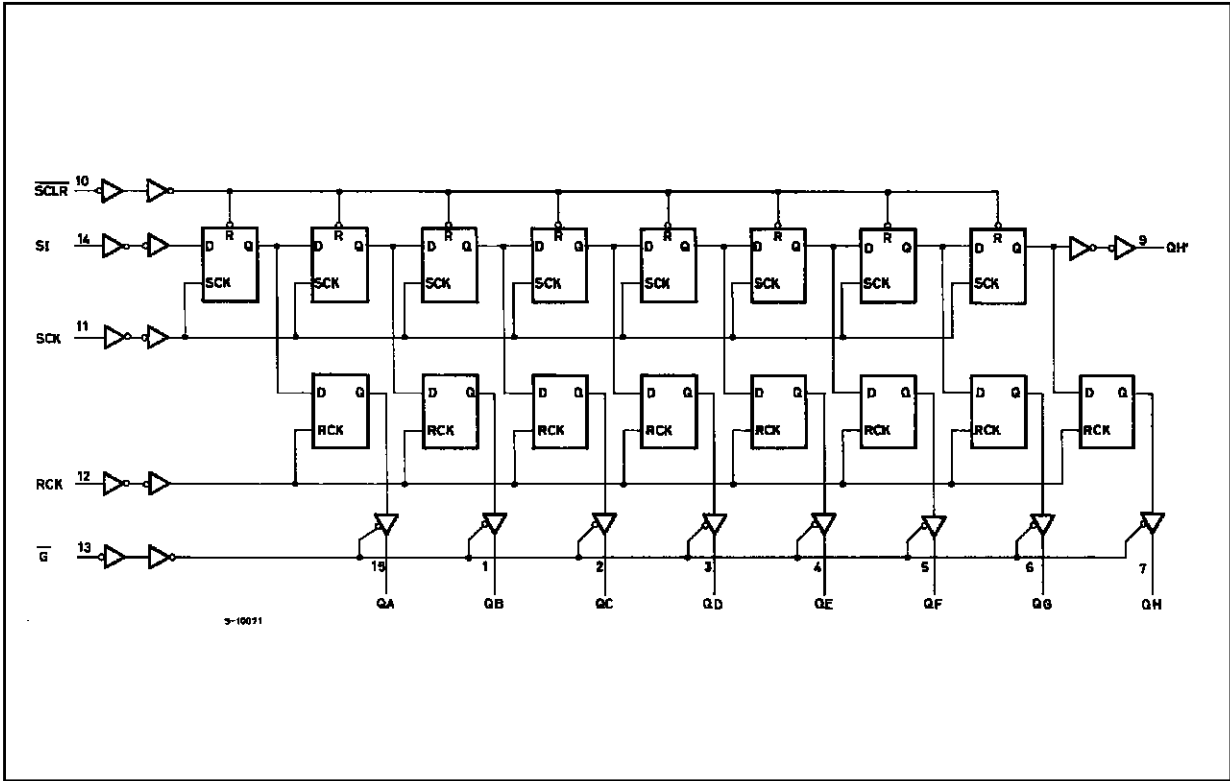
INPUTS					OUTPUT
SI	SCK	$\overline{\text{SCLR}}$	RCK	$\overline{\text{G}}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L		H	X	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H		H	X	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X		H	X	X	STATE OF S.R IS NOT CHANGED
X	X	X		X	S.R. DATA IS STORED INTO STORAGE REGISTER
X	X	X		X	STORAGE REGISTER STATE IS NOT CHANGED

X: DONT CARE

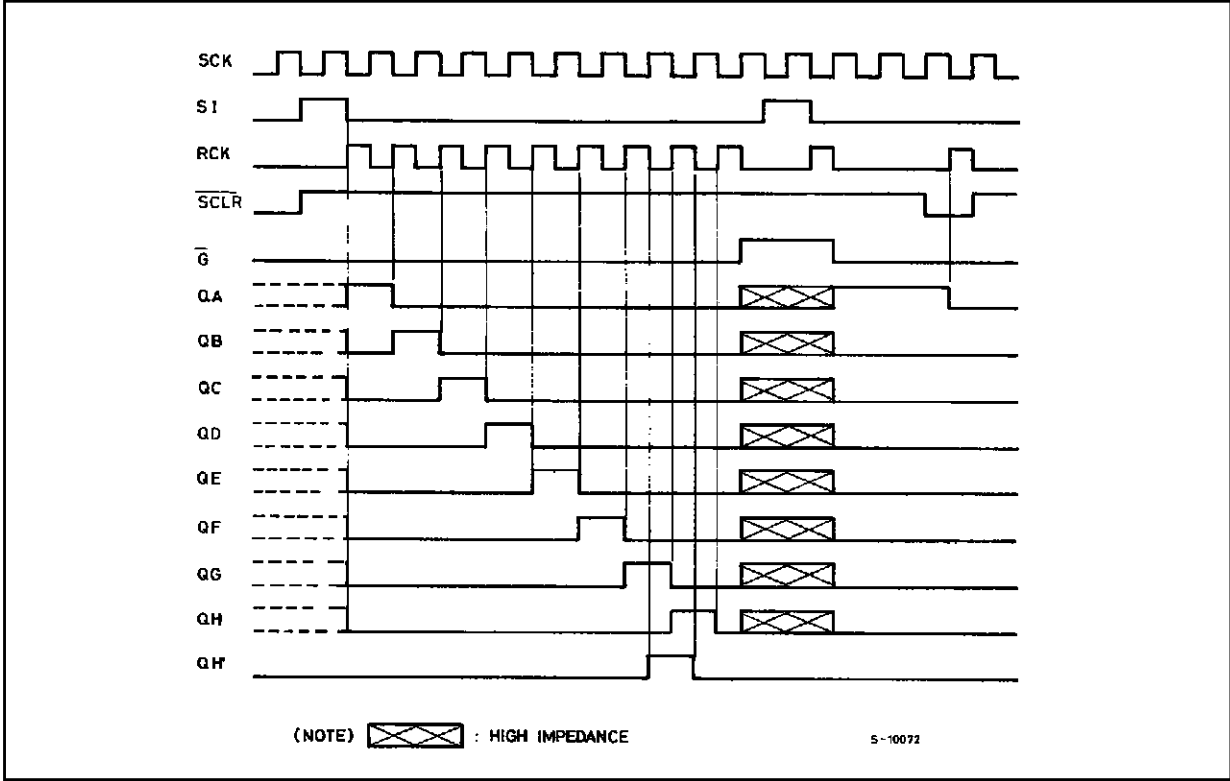
LOGIC DIAGRAM



LOGIC DIAGRAM



TIMING CHART

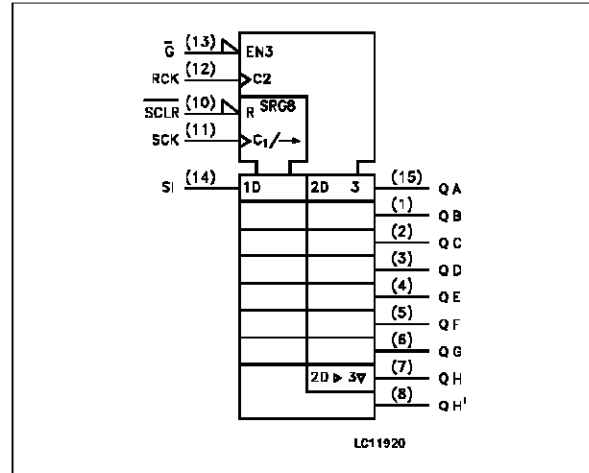


M54/M74HC595

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Data Outputs
9	QH'	Serial Data Outputs
10	SCLR	Shift Register Clear Input
11	SCK	Shift Register Clock Input
13	\bar{G}	Output Enable Input
14	SI	Serial Data Input
12	RCK	Storage Register Clock Input
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current Per Output Pin QA-QH	± 35	mA
I _O	DC Output Current Per Output Pin QH'	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ± 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage (for QH' output)	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I _O = -5.2 mA	5.68	5.8		5.63		5.60		
V _{OH}	High Level Output Voltage (for QA to QH outputs)	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O = -6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I _O = -7.8 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage (for QH' output)	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I _O = 5.2 mA		0.18	0.26		0.33		0.40	
V _{OL}	Low Level Output Voltage (for QA to QH outputs)	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I _O = 7.8 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{OZ}	3 State Output Off State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.5		±5		±10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

M54/M74HC595

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

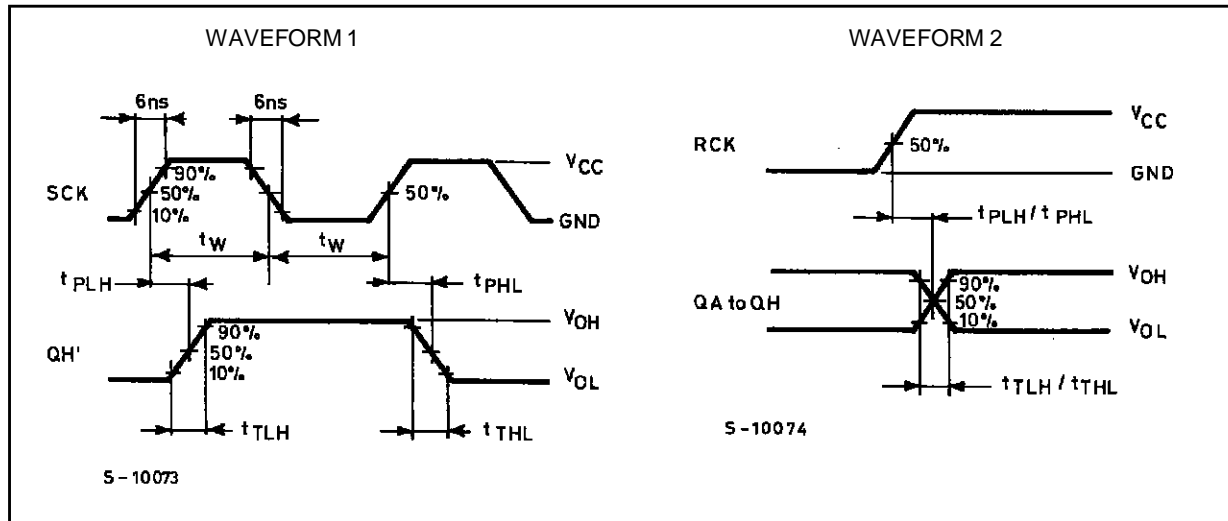
Symbol	Parameter	Test Conditions			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time (Qn)	2.0	50		25	60		75		90	ns	
		4.5		7	12		15		18			
		6.0		6	10		13		15			
t _{TLH} t _{THL}	Output Transition Time (QH')	2.0	50		30	75		95		115	ns	
		4.5		8	15		19		23			
		6.0		7	13		16		20			
t _{PLH} t _{PHL}	Propagation Delay Time (SCK - QH')	2.0	50		45	125		155		190	ns	
		4.5		15	25		31		38			
		6.0		13	21		26		32			
t _{PLH} t _{PHL}	Propagation Delay Time (SCLR - QH')	2.0	50		60	175		220		265	ns	
		4.5		18	35		44		53			
		6.0		15	30		37		45			
t _{PLH} t _{PHL}	Propagation Delay Time (RCK - Qn)	2.0	50		60	150		190		225	ns	
		4.5		20	30		38		45			
		6.0		17	26		32		38			
		2.0	150		75	190		240		285	ns	
		4.5		25	38		48		57			
		6.0		22	32		41		48			
t _{PZL} t _{PZH}	3 State Output Enable Time	2.0	50	R _L = 1 KΩ	45	135		170		205	ns	
		4.5			15	27		34		41		
		6.0			13	23		29		35		
		2.0	150	R _L = 1 KΩ	60	175		220		265	ns	
		4.5			20	35		44		53		
		6.0			17	30		37		45		
t _{PLZ} t _{PHZ}	3 State Output Disable Time	2.0	50	R _L = 1 KΩ	30	150		190		225	ns	
		4.5			15	30		38		45		
		6.0			14	26		32		38		
f _{MAX}	Maximum Clock Frequency	2.0	50		6.0	17		4.8		4	ns	
		4.5		30	50		24		20			
		6.0		35	59		28		24			
		2.0	150		5.2	14		4.2		3.4	ns	
		4.5		26	40		21		17			
		6.0		31	45		25		20			
t _{W(H)}	Minimum Pulse Width (SCK, RCK)	2.0	50		17	75		95		110	ns	
		4.5		6	15		19		22			
		6.0		6	13		16		19			
t _{W(L)}	Minimum Pulse Width (SCLR)	2.0	50		20	75		95		110	ns	
		4.5		6	15		19		22			
		6.0		6	13		16		19			
t _s	Minimum Set-up Time (SI - CCK)	2.0	50		25	50		65		75	ns	
		4.5		5	10		13		15			
		6.0		4	9		11		13			

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

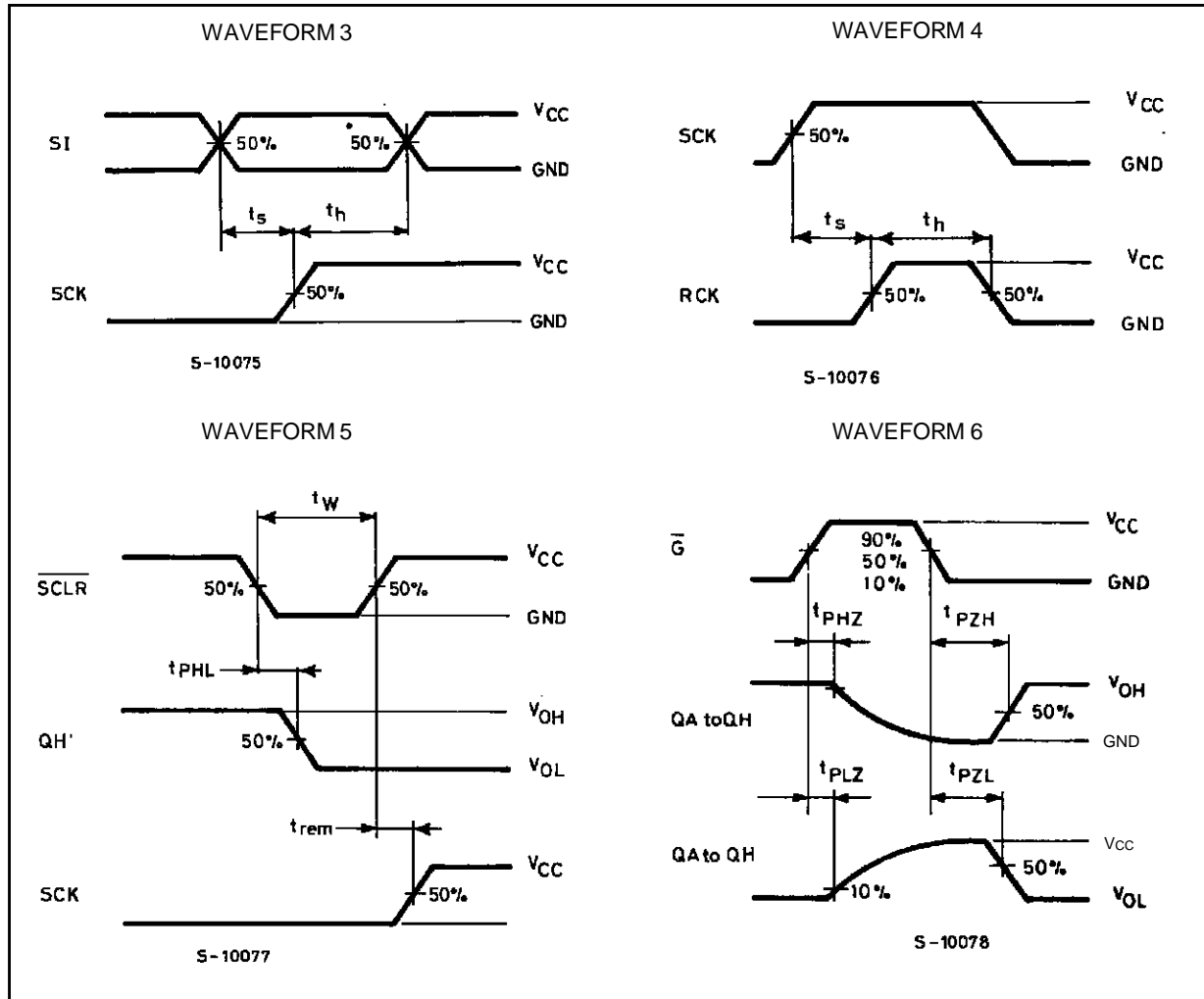
Symbol	Parameter	Test Conditions			Value						Unit
		V_{CC} (V)	C_L (pF)	$T_A = 25 \text{ }^\circ\text{C}$ 54HC and 74HC			$-40 \text{ to } 85 \text{ }^\circ\text{C}$ 74HC		$-55 \text{ to } 125 \text{ }^\circ\text{C}$ 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Set-up Time (SCK - RCK)	2.0	50		35	75		95		110	ns
		4.5		8	15		19		22		
		6.0		6	13		16		19		
t_s	Minimum Set-up Time (SCRL - RCK)	2.0	50		40	100		125		145	ns
		4.5		10	20		25		29		
		6.0		7	17		21		25		
t_h	Minimum Hold Time	2.0	50			0		0		0	ns
		4.5			0		0		0		
		6.0			0		0		0		
t_{REM}	Minimum Clear Removal Time	2.0	50		15	50		65		75	ns
		4.5		3	10		13		15		
		6.0		3	9		11		13		
C_{IN}	Input Capacitance				5	10		10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance				184						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

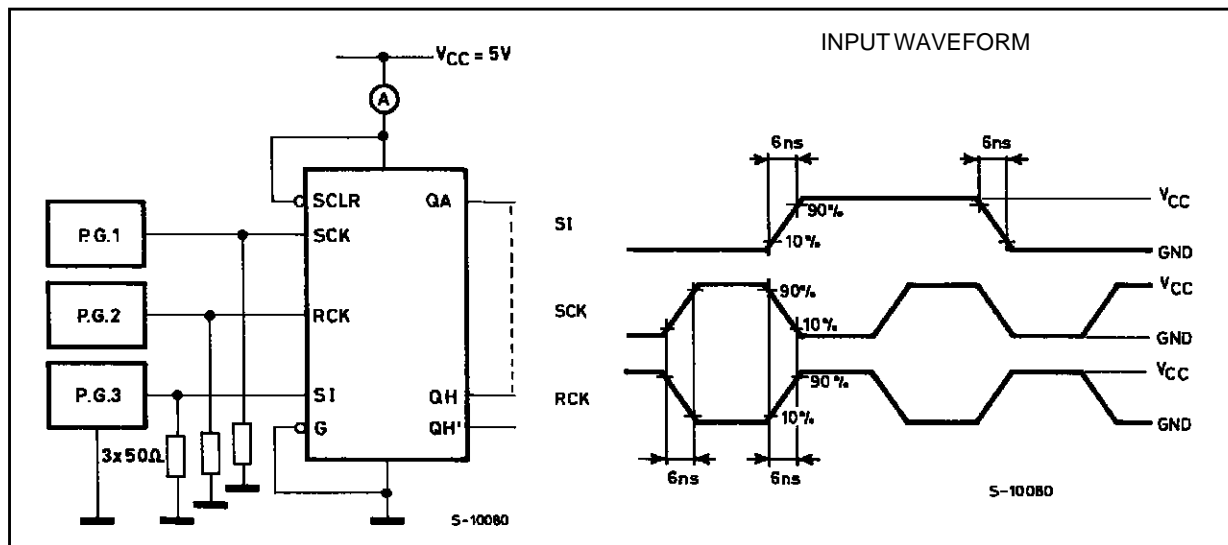
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)



TEST CIRCUIT I_{CC} (Opr.)



Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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