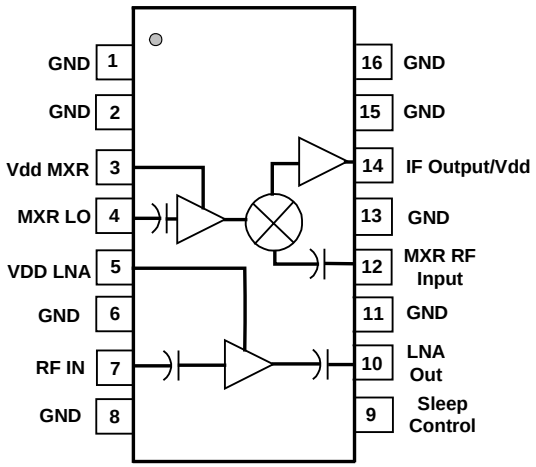
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ5122

DATA SHEET

3V Cellular TDMA/AMPS Receiver IC With Power-Down



Features

- *Power-Down, "Sleep" Mode*
- *Single 2.8V operation*
- *Low-current operation*
- *Small QSOP-16 plastic package*
- *Few external components*

Applications

- *IS-136 TDMA Mobile Phones*
- *Dual Mode TDMA/AMPS Mobile Phones*
- *AMPS Mobile Phones*

Product Description

The TQ5122 is a 3V, RF receiver IC designed specifically for Cellular band TDMA applications. It's RF performance meets the requirements for products designed to the IS-136 TDMA and the AMPS standards. The TQ5122 includes a power–down mode which allows current saving during standby and the non-operating portion of the TDMA pulse. The TQ5122 contains LNA and Mixer circuits matched to the 800MHz cellular band.

The mixer uses a high-side LO frequency. The IF has a usable frequency range of 85 to 150MHz. The LNA Output and Mixer Input ports are internally matched to simplify the design and keep the number of external components to a minimum. The TQ5122 achieves excellent RF performance with low current consumption which yields long standby times in portable applications. The small QSOP-16 package is ideally suited for Cellular band mobile phones.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Frequency	869		894	MHz
Gain		18.5		dB
Noise Figure		2.7		dB
Input 3rd Order Intercept		-8.5		dBm
DC supply Current		12.0		mA

Note 1: Test Conditions: Vdd=2.8VDC, Tc=25°C, Filter IL=2.5dB, RF=881MHz, LO=1016MHz, IF=135MHz, LO input=-7dBm

Electrical Characteristics[1,2]

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency		869		894	MHz
LO Frequency		954		1044	MHz
IF Frequency		85		150	MHz
LO input level		-7	-4	0	dBm
Supply voltage		2.7	2.8	4.0	V
Gain		16.0	18.5		dB
Gain Variation vs. Temp.	-40 to 85 °C			+/-2.0	dB
Noise Figure			2.7	3.5	dB
Input 3rd Order Intercept		-11.0	-8.5		dBm
Return Loss	LNA input – with external match	10			dB
	LNA output	10			dB
	Mixer RF input	10			dB
	Mixer LO input	10			dB
Isolation	LO to LNA RF in	35			dB
	LO to IF; after IF match		40		dB
	RF to IF; after IF match		20		dB
IF Output Impedance	Vdd = 2.8V; Sleep mode, Device On		500		Ohm
	Vdd = 2.8V; Sleep mode, Device Off		Approx. Open		Ohm
	Vdd = 0V		<50		Ohm
Power Down, “sleep”	Device On Voltage		Vdd	Vdd	VDC
	Device Off Voltage	0	0		VDC
Supply Current, Sleep mode, Device On	Tc = + 25 °C		12	15	mA
Supply Current, Sleep mode, Device Off	Enable voltage = 0, LO Drive off		100	1000	µA
Operating Temperature, case		-40	25	+85	°C

Note 1: Test Conditions: Vdd=2.8VDC, Filter IL=2.5dB, RF=881MHz, LO=1016MHz, IF=135MHz, LO input=-7dBm, T_C = 25°C, unless otherwise specified.
Note 2: Min./Max. limits are at +25°C case temperature unless otherwise specified.

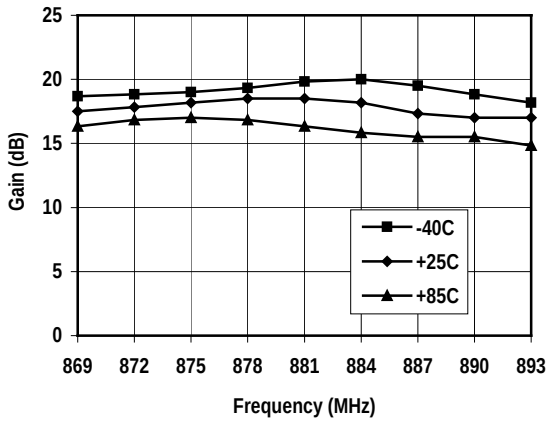
Absolute Maximum Ratings

Parameter	Value	Units
DC Power Supply	5.0	V
Power Dissipation	500	mW
Operating Temperature	-55 to 100	°C
Storage Temperature	-60 to 150	°C
Signal level on inputs/outputs	+20	dBm
Voltage to any non supply pin	-0.3 to Vdd + 0.3	V

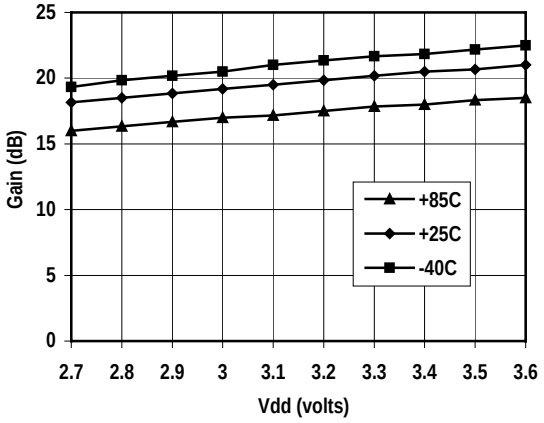
Typical Performance

Test Conditions (Unless Otherwise Specified): Vdd=2.8VDC, Tc=25°C, filter IL=2.5dB, RF=881MHz, LO=1016MHz, IF=135MHz, LO input=-7dBm

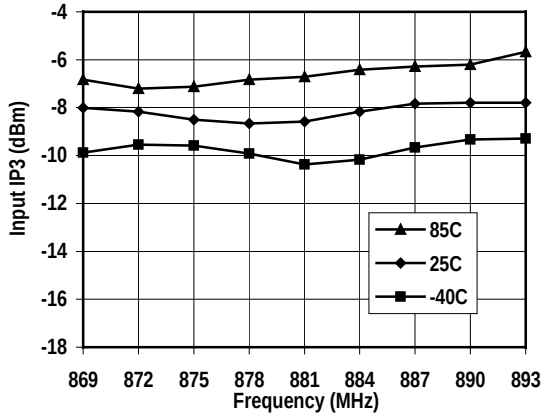
Gain vs. Frequency vs. Temperature



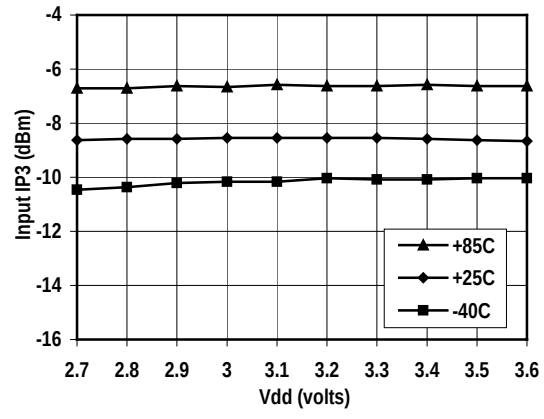
Gain vs. Vdd vs. Temperature



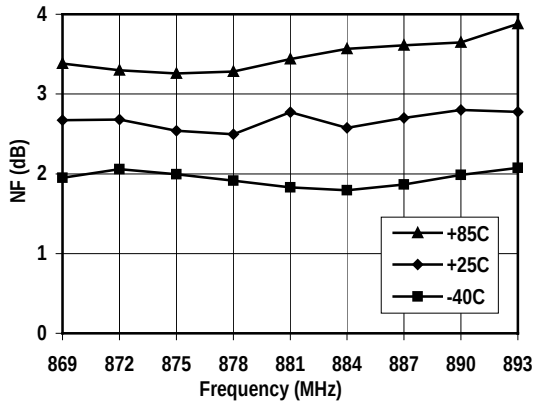
Input IP3 vs. Frequency vs. Temperature



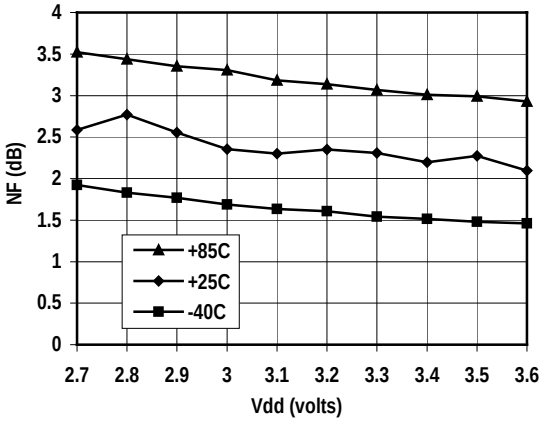
Input IP3 vs. Vdd vs. Temperature



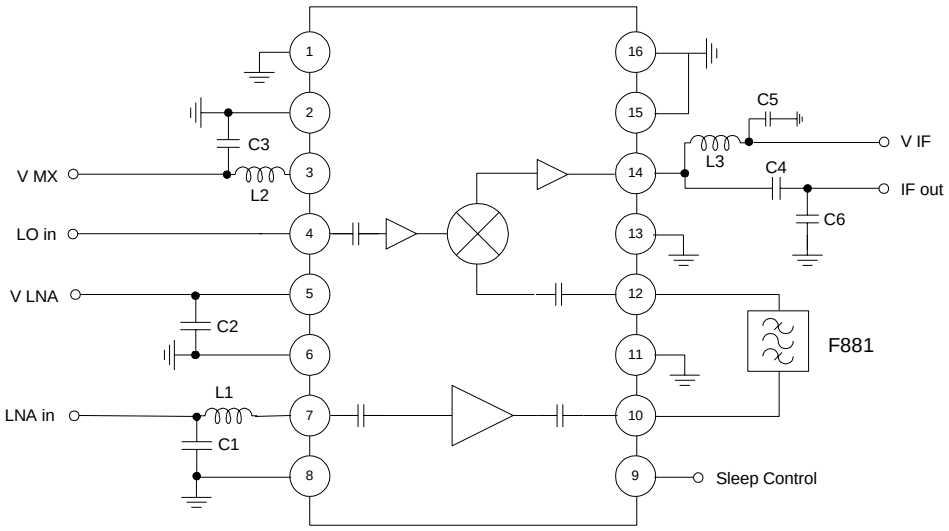
NF vs. Frequency vs. Temperature



NF vs. Vdd vs. Temperature



Application/Test Circuit



Bill of Material for TQ5122 Receiver Application/Test Circuit*

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC	U1	TQ5122		QSOP-16	TriQuint Semiconductor
Capacitor	C1		2.7pF	0603	
Capacitor	C2, C3		22pF	0603	
Capacitor	C4		10pF	0603	
Capacitor	C5		1000pF	0603	
Capacitor	C6		8.2 pF	0603	
Inductor	L1		22nH	0603	
Inductor	L2		12nH	0603	
Inductor	L3		150nH	0805	
Toyocom (select)	F1	T726881A	627-881A		Toyocom

* May vary due to printed circuit board layout and material.

TQ5122 Product Description

The TQ5122 3V RFIC Downconverter is designed specifically for cellular band TDMA/AMPS applications. The TQ5122 contains LNA, Mixer and LO buffer circuits matched to the 800 MHz cellular frequency band. The IF frequency may be selected between 85 and 150 MHz. Most RF ports are internally matched to 50 Ω simplifying the design and minimizing the number of external components. The TQ5122 also includes a power–down mode switch which allows current saving during standby and the non-operating portion of the TDMA pulse.

Operation

Please refer to the test circuit above.

Low Noise Amplifier (LNA)

The LNA section of the TQ5122 are cascaded common source FET's, see Figure 1. It is designed to operate on DC supply voltages from 2.7V to 5V. The source terminal must be grounded as close as possible to Pin 8 to avoid significant gain reduction due to degeneration. The LNA requires an input matching circuit to obtain best noise figure, gain and return loss. The LNA output is close to 50 Ω for direct connection to a 50 Ω image reject filter.

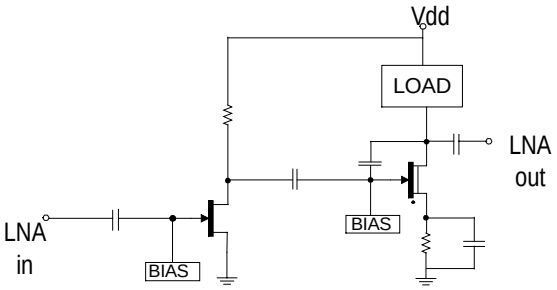


Figure 1. Simplified Schematic of LNA Section

LNA Input Match

The designer can make some Noise Figure and Gain trade off by varying the off chip LNA input matching circuit values and topology. This allows the TQ5122 to be optimized for specific system requirements.

The LNA gain, noise figure and input return loss are a function of the source impedance (Z_s), or reflection coefficient (Γ_s), presented to the input pin. Highest gain and lowest return loss occur when Γ_s is equal to the complex conjugate of the LNA input impedance. A different source reflection coefficient, Γ_{opt}, which is experimentally determined, will provide the lowest noise figure, F_{min}.

The noise resistance, R_n, provides an indication of the sensitivity of the noise performance to changes in Γ_s as seen by the LNA input.

$$F_{LNA} = F_{MIN} + \frac{4R_N}{Z_0} \cdot \frac{|\Gamma_{opt} - \Gamma_S|^2}{|1+\Gamma_{opt}|^2 \cdot \left(1-|\Gamma s|^2\right)}$$

Components such as filters and mixers placed after the LNA degrade the overall system noise figure according to the following equation:

$$F_{SYSTEM} = F_{LNA} + \frac{F_2 - 1}{G_{LNA}}$$

F_{LNA} and G_{LNA} represent the linear noise factor and gain of the LNA and F_2 is the noise factor of the next stage. The system noise figure is a compromise between the highest gain and minimum noise figure of the LNA. See Table 1 for noise parameters.

Table 1. TQ5122 Noise Parameters

Freq. MHz	|Gopt|	∠Gopt	Fmin	Rn
830	0.88	34.5	0.75	51.2
880	0.83	37.8	0.89	50.4
930	0.82	40.0	0.97	50.0

LNA Output Match

The output impedance of the LNA was designed for 50Ω. The internal 50Ω match eliminates the need for external components at this port. It also improves IP3 performance and power gain.

The output of the LNA is intended to be connected directly to an image reject filter. Depending on the filter, additional components may be needed to better match to the LNA output. Some image reject filters may require a series inductor to smooth the frequency response and improve overall performance.

Mixer

The mixer of the TQ5122 uses a common source depletion mode MESFET. The mixer is designed to operate on supply voltages from 2.7V to 5V. A 50Ω matched on-chip buffer amplifier allows direct connection of the LO input to commercially available VCO's with output drive levels down to -7dBm. The common-gate LO buffer provides good input match and supplies the voltage gain needed to drive the mixer FET. The mixer also has an "*open-drain*" IF output which provides flexibility in matching to various IF frequencies and filter impedances, see Figure 2.

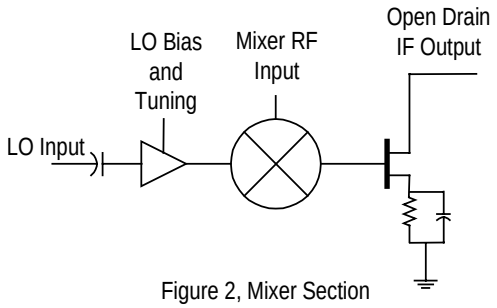


Figure 2, Mixer Section

LO Input Port

The LO input port is matched to 50Ω. This allows the TQ5122 to operate at low LO drivel levels. However, the values and positions of L2 and C3 shown in the applications circuit effect the gain of the LO buffer amplifier and are important to the proper operation of the TQ5122. See "Calculation of nominal L2 Value" below

The common gate buffer amplifier provides the voltage gain needed to drive the gate of the mixer FET while using very little current (approximately 1.5mA).

Because of the 50Ω input match of the buffer amplifier and the internal DC blocking capacitor, the system VCO output can be directly connected to the TQ5122 LO input via a 50Ω transmission line with no additional components.

Mixer Input

Although the mixer input port is matched to 50Ω, TriQuint has found that LO leakage through the Mixer RF input pin, can in some cases, reflect off the SAW image reject filter and return back to the mixer out of phase. This may cause some degradation in conversion gain and system noise figure. Sensitivity to the phenomena depends on the particular filter model and the line length between the mixer input pin and the filter. In some cases a small inductance can be added between the filter and the mixer input to compensate. With some line lengths and filter combinations, no inductor is necessary.

LO Buffer & Calculation of Nominal L2 Value

The node between the LO buffer amplifier and the mixer FET is brought out to Pin 3 (V MX) and connected by an inductor to AC ground. This inductor is selected to resonate with internal on chip capacitance at the LO frequency in order to reduce out-of-band gain and improve noise performance.

The internal capacitance of the LO amplifier output plus the stray capacitance on the board surrounding Pin 3 is approximately 1.5 pF. The inductor is selected to resonate with the total capacitance at the LO frequency using the following equation:

$$L = \frac{1}{C(2\Pi f)^2}, where \cdot C = 1.5\,pF$$

The final values must be confirmed with measurements on a board approximating the final layout. The final layout will affect the value and position of L2 and its bypass capacitor, C3, see Figure 5.

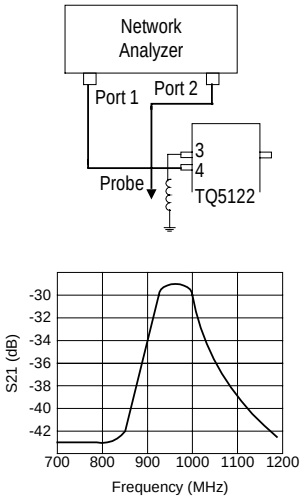


Figure 3. LO Buffer Frequency Response

Measuring the LO Frequency Response

The frequency response of the LO driver amplifier can be measured using a semi-rigid probe, see Figure 3, and a network analyzer.

Connect port 1 to the LO input (Pin 4) of the TQ5122 with the source power set to deliver -7 dBm. Connect the coaxial probe to Port 2 and place the probe tip approximately 0.1 inch away from either Pin 3 or the inductor.

If the calculated shunt inductor (L2) is not a standard value, the AC ground bypass capacitor C3 can be positioned along the transmission line to adjust for the right inductance, see Figure 4. Once this is completed, the peak of the response should be centered at the center of the LO frequency band.

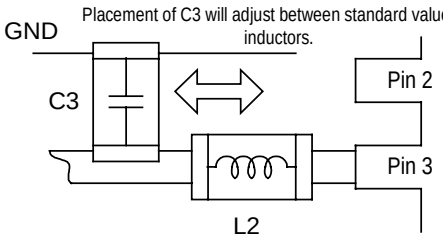


Figure 4, Adjusting the AC Ground

Mixer IF Port

The Mixer IF output is an "open-drain" configuration, allowing for flexibility in efficient matching to various filter types and at various IF frequencies.

For evaluation of the LNA and mixer, it is usually necessary to impedance match the IF port to the 50Ω test systems. When verifying or adjusting the matching circuit on the prototype circuit board, the LO drive should be injected at pin 4 at the nominal power level of -4 dBm, since the LO level does have an impact on the IF port impedance.

There are several networks that can be used to properly match the IF port to the SAW or crystal IF filter. The mixer supply voltage is applied through the IF port, so the matching circuit topology must contain either an RF choke or shunt inductor. An extra DC blocking capacitor is not necessary if the output will be attached directly to a SAW or crystal bandpass filters.

Figure 5 illustrates a shunt L, series C, shunt C IF matching network. It is one of the simplest matching networks and requires the fewest components. DC current can be easily injected through the shunt inductor and the series C provides a DC block, if needed. The shunt C, is used to reduce the LO leakage.

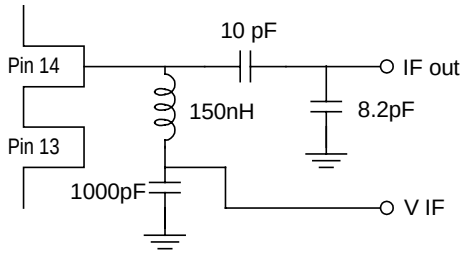


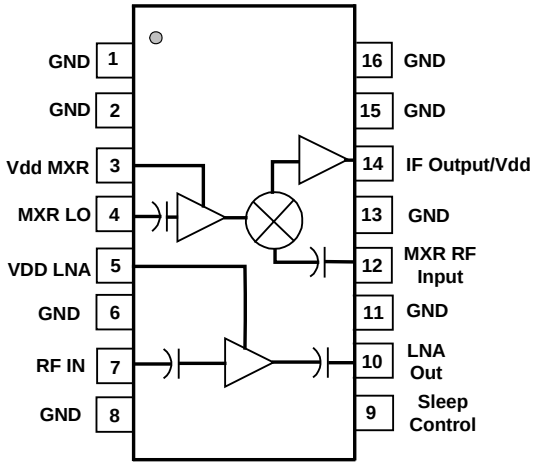
Figure 5, IF Output Match, 135 MHz

Power down, "sleep" mode

The power down circuit is used to reduce average power consumption in TDMA applications by toggling the receiver on and off within the receive time slot when no signal is present.

The power down circuitry operates through the incorporation of enhancement-mode FET switches in all DC paths. Level shifting circuitry is incorporated for the purpose of providing an interface compatible with CMOS logic levels. The entire chip nominally draws 100uA when the power-down pin is at 0V. When the power-down pin is at 2.8V (Vdd), the chip draws nominal specified current. The power-down pin itself, Pin 9, draws approximately 40uA when 2.8V is applied. Less than 1uA is sourced from the power-down pin when 0V is applied.

Package Pinout

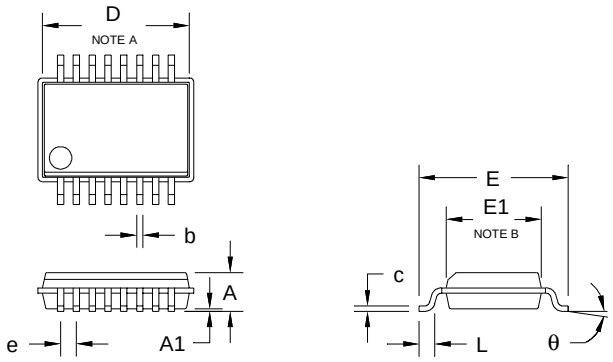


Pin Descriptions

Pin Name	Pin #	Description and Usage
GND	1	Ground
GND	2	Ground
VDD_MXR	3	Mixer LO buffer supply voltage. Series inductor required for LO buffer tuning. Local external bypass capacitor required.
MXR LO IN	4	Mixer LO input. DC blocked, matched to 50Ω
V_{DD} LNA	5	LNA DC supply voltage. Local external bypass capacitor required.
GND	6	Ground
LNA IN	7	LNA RF input. DC blocked. Requires external matching elements for noise match and match to 50Ω
GND, LNA	8	LNA first stage ground connection. Direct connection to ground required.
SLEEP	9	Power-Down mode control.
LNA OUT	10	LNA RF output. DC blocked. Matched to 50Ω.
GND	11	Ground
MXR_RF	12	Mixer RF input, DC blocked. Matched to 50Ω.
GND	13	Ground
IF OUT	14	IF output. Open drain output, connection to Vdd required. External matching is required.
GND	15	Ground
GND	16	Ground

For ground pins 1, 2, 6, 11, 13, 15, and 16, TriQuint recommends use of several via holes to the backside ground immediately adjacent to the pin.

Package Type: Power QSOP-16 Plastic Package



DESIGNATION	DESCRIPTION	ENGLISH		METRIC		NOTE
A	OVERALL HEIGHT	0.064	+/-.005 in	1.63	+/-.13 mm	C
A1	STANDOFF	0.007	+/-.003 in	0.18	+/-.08 mm	C
b	LEAD WIDTH	0.010	+/-.002 in	0.25	+/-.05 mm	C
c	LEAD THICKNESS	0.085	+/-.015 in	2.16	+/-.38 mm	C
D	PACKAGE LENGTH	0.193	+/-.004 in	4.90	+/-.10 mm	A, C
e	LEAD PITCH	0.025	BSC	0.635	BSC	
E	LEAD TIP SPAN	0.236	+/-.008 in	5.99	+/-.20 mm	C
E1	PACKAGE WIDTH	0.154	+/-.003 in	3.91	+/-.08 mm	B, C
L	FOOT LENGTH	0.033	+/-.017 in	0.84	+/-.43 mm	C
θ	FOOT ANGLE	4	+/-4 DEG	4	+/-4 DEG	

NOTES:

A. The D dimension does not include mold flashing and mismatch. Mold flashing and mismatch shall not exceed .006 in (.15 mm) per side.

B. The E1 dimension does not include mold flashing and mismatch. Mold flashing and mismatch shall not exceed .010 in (.25 mm) per side.

C. Primary units are English inches. The metric equivalents are subject to rounding error.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: info_wireless@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

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