DOT MATRIX LCD 64-OUT SEGMENT DRIVER

■ GENERAL DESCRIPTION

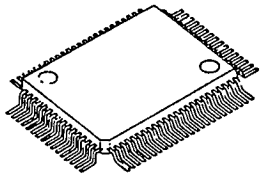
The NJU6417C is a serial input, 64-out segment driver for dot matrix LCDs, especially useful as extension driver for LCD controller drivers like NJU6408B.

It consists of 64-bit (two of 32-bit) shift register, 64-bit latch, and 64 high voltage LCD drivers.

The shift direction of each 32-bit shift register can be set independently to each other, consequently the efficient extension driver allocation according to the number of characters and easy wiring with the LCD panel can be performed.

As the 64-driver have 4 level voltage inputs to drive the LCD, adjustable driving voltage according to the LCD panel can be supplied from the external power source.

■ PACKAGE OUTLINE

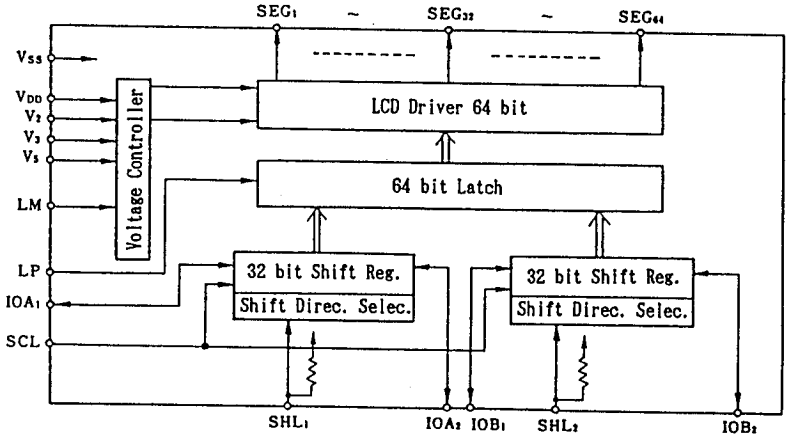


NJU6417CF

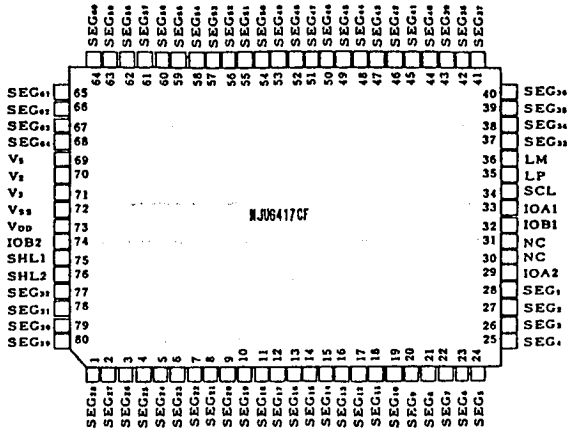
■ FEATURES

- 64 Segment Drivers
- 64-bit Shift Register
  (Two of 32-bit Shift Registers)
- Shift Direction of each 32-bit
  Shift Registers Selection
- Two of Shift Direction Select Terminal
- Duty Ratio 1/8 to 1/16
- Fast Data Transmission (Shift Clock 6 MHz max.)
- External Power Supply for LCD Driving Voltage
- LCD Driving Voltage --- V_{DD} - 3V ~ V_{DD} - 13.5V
- Operating Voltage --- 5 V ± 10 %
- Package Outline --- QFP 80
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N
1～28 37～68 77～80	SEG_1～ SEG_{64}	LCD segment driving terminal. Each terminal corresponds to each bit of shift register
29 33	IOA_2 IOA_1	Data input/output terminals for 1st to 32nd bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL_1 terminal.
32 74	IOB_1 IOB_2	Data input/output terminals for 33rd to 64th bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL_2 terminal.
34	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time (T_{RS}) and falling time (T_{FS}) should be set less than 50ns respectively.
35	LP	Latch pulse input terminal. The data in the shift register is latched to the Latch by this signal. "H" : Data writing, "L" : Data latch
36	LM	Alternate signal input for LCD driving.
69, 71 70	V_5, V_3 V_2	LCD driving power source terminals. $V_{DD} \geqq V_2 \geqq V_3 \geqq V_5$, $V_{DD} \geqq V_{SS} \geqq V_5$
72 73	V_{DD} V_{SS}	Power supply terminal (connect to the controller's V_{DD} terminal) Power supply terminal (connect to the controller's V_{SS} terminal)
75	SHL_1	Shift direction and input/output control terminal(Pull-up R). "H" or Open : Shift direction is from 1st bit to 32nd bit. "L" : Shift direction is from 32nd bit to 1st bit.
76	SHL_2	Shift direction and input/output control terminal(Pull-up R). "H" or Open : Shift direction is from 33rd bit to 64th bit. "L" : Shift direction is from 64th bit to 33rd bit.
54	NC	Non connection.

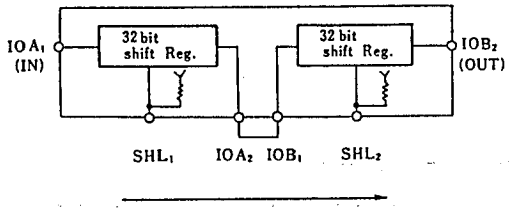
■ FUNCTIONAL DESCRIPTION

(1) Shift register control

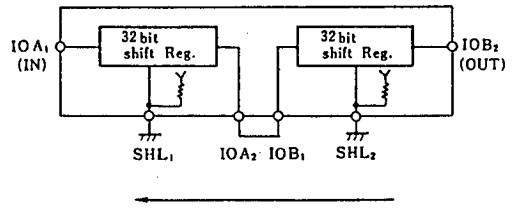
The 64-bit shift register is divided into two of 32-bit shift register.
The shift direction of each 32-bit shift register can be set independently to each other shown in below.

Control Terminal	Input	Shift Direction
SHL_1	"H" or Open	$IOA_1 \rightarrow IOA_2$
	"L"	$IOA_1 \leftarrow IOA_2$
SHL_2	"H" or Open	$IOB_1 \rightarrow IOB_2$
	"L"	$IOB_1 \leftarrow IOB_2$

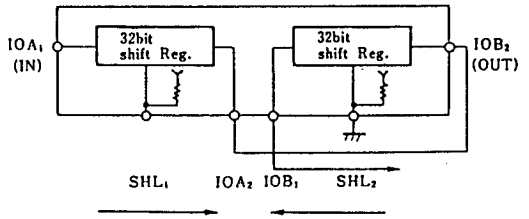
(1−1) When the terminals SHL_1 and SHL_2 are "H" or open, the data shift from SEG_1 to SEG_{64}.



(1−2) When the terminals SHL_1 and SHL_2 are "L", the data shift from SEG_{64} to SEG_1.



(1−3) Reversed sift direction to each other is also available.
$SEG_1 \rightarrow SEG_{32} \rightarrow SEG_{64} \rightarrow SEG_{33}$ example is shown in below:



(2) LCD driver output truth table.

Input Data	Selection/Non-selection	LM	Driver Output (SEG_1 to SEG_{64})
"H"	Selection	H	V_5
		L	V_{DD}
"L"	Non-selection	H	V_3
		L	V_2

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Supply Voltage (2) Note 1)	V_{DD} ~ V_5	V_{DD}-13.5 ~ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	℃
Storage Temperature	Tstg	- 55 ~ + 150	℃

Note 1) The relation : $V_{DD} \geqq V_2 \geqq V_3 \geqq V_5$ must be maintained.

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■ ELECTRICAL CHARACTERISTICS

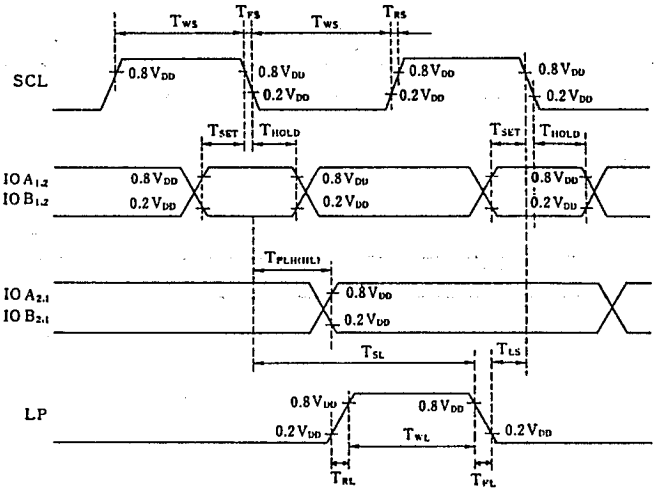
• DC Characteristics

(V_{DD}=5V±10% , Ta=-20 ~ +75℃)

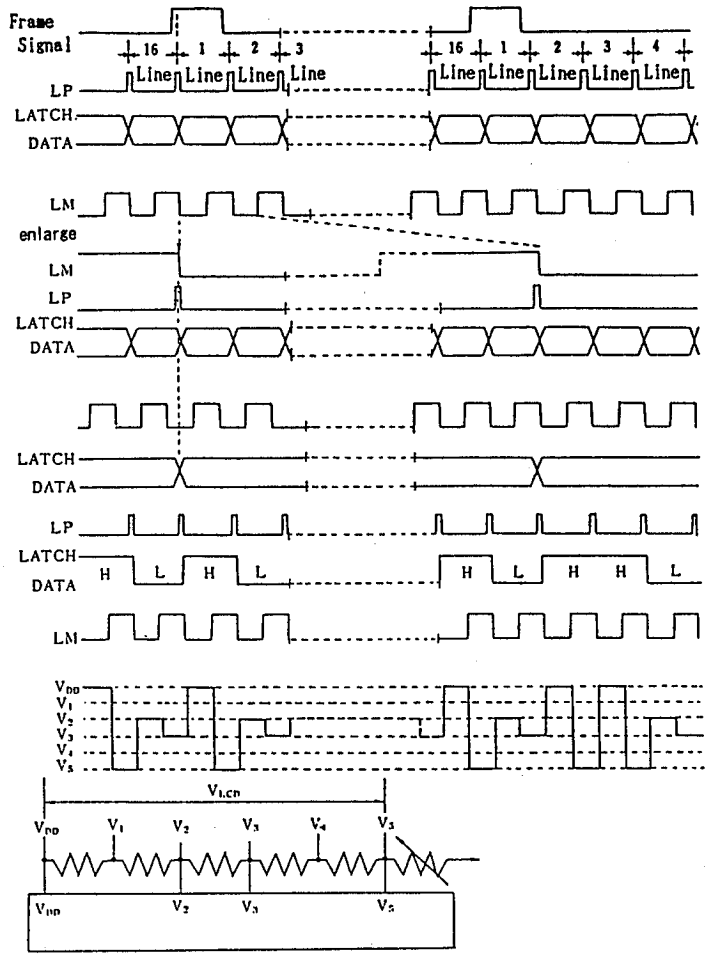
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage	V_{IH}	LM, LP, SHL_1, SHL_2 Terminals		0.8V_{DD}		V_{DD}	V
	V_{IL}					0.2V_{DD}	
Input Current	I_{IH1}	V_{IH}=V_{DD}	LM, LP Terminals			1	uA
	I_{IL1}	V_{IL}=0V				- 1	
	I_{IH2}	V_{IH}=V_{DD}	SHL_1, SHL_2 Terminals			1	
	I_{IL2}	V_{IL}=0V		- 10	- 15	- 25	
Output Voltage	V_{OH}	I_O=- 40uA	OA_1, OA_2, OB_1, OB_2 Terminals	4.2			V
	V_{OL}	I_O= 400uA				0.4	
Driver On-resistance	R_{ON}	Id=0.05mA	SEG_1 ~ SEG_{64} Terminals			30	kΩ
Operating Current (Logic Part)	I_{SSO}	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.			0.85	1.2	mA
Operating Current (LCD Driver Part)	I_{SSHO}	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.			70	100	uA
LCD Driving Voltage	V_{LCD}	V_{DD} - V_5		V_{DD}-3.0		V_{DD}-13.5	V

• AC Characteristics

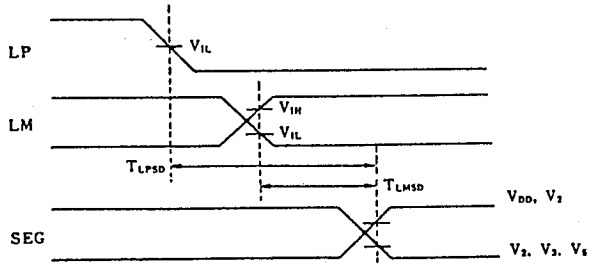
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$T_{PLH(HL)}$				150	ns
Maximum Operating Frequency	f_{SCL}	Duty = 50 %			6	MHz
SCL Pulse Width	T_{WS}		63			ns
LP Pulse Width	T_{WL}		110			ns
Set up Time	T_{SET}		50			ns
SCL → LP Time	T_{SL}		100			ns
LP → SCL Time	T_{LS}		0			ns
Data Hold Time	T_{HOLD}		30			ns
SCL Rise, Fall Time	T_{RS}, T_{FS}				50	ns
LP Rise, Fall Time	T_{RL}, T_{FL}				1	us



■ TIMING CHART 1/5 Bias, 1/16 Duty Ratio



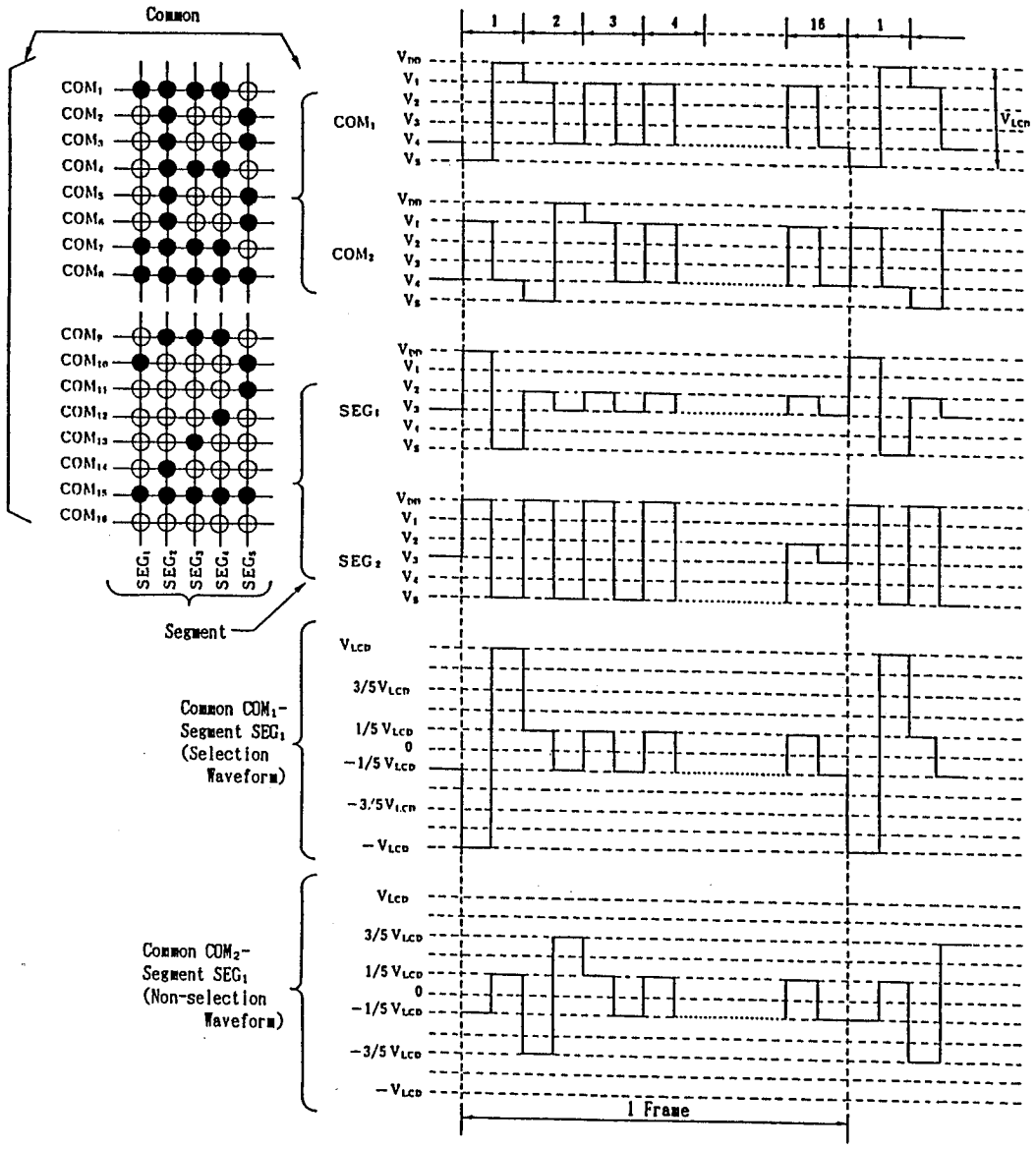
■ SEGMENT SIGNAL OUTPUT TIMING



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP - SEG Output Delay Time	T_{LPSD}	C_L = 100pF			4.5	us
LM - SEG Output Delay Time	T_{LMSD}	C_L = 100pF			4.5	

■ LCD DRIVING WAVEFORM EXAMPLE

1/5 Bias, 1/16 Duty Ratio



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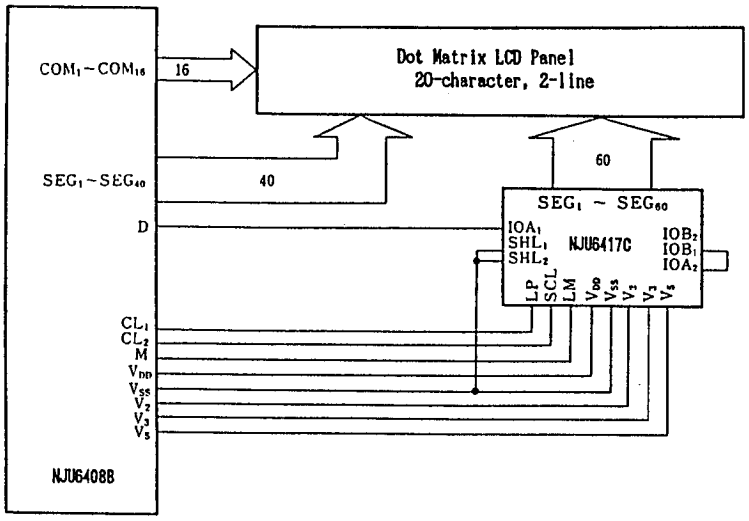
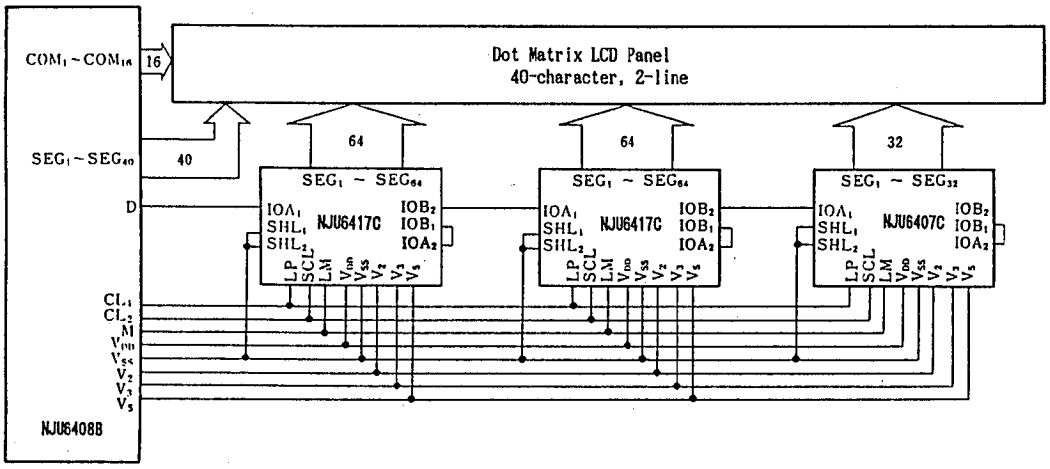
■ APPLICATION CIRCUITS

(1) 20-character 2-line Display Example (Combine with NJU6408B)



(2) 40-character 2-line Display Example (NJU6408B + NJU6417C x 2 + NJU6407C)



MEMO