

### Description

The WM8143-12 integrates the analogue signal conditioning required by CCD sensors with a 12-bit ADC. The WM8143-12 requires minimal external circuitry and provides a cost-effective sensor to digital domain system solution.

Each of the three analogue conditioning channels includes reset level clamp, CDS, fine offset level shifting and programmable gain amplification. The three channels are multiplexed into the ADC. The output from the ADC is fed to the output bus pins OP[11:0] via a 12/8 bit multiplexer, enabled by the OEB signal.

The flexible output architecture allows twelve-bit data to be accessed either on a twelve-bit bus or via a time-multiplexed eight-bit bus. The WM8143-12 can be configured for pixel-by-pixel or line-by-line multiplexing operation. Reset level clamp and/or CDS features can be optionally bypassed. The device configuration is programmed either via a simple serial interface or via an eight-bit parallel interface.

The serial/parallel interfaces of the WM8143-12 are control compatible with those of the WM8144-10 and WM8144-12.

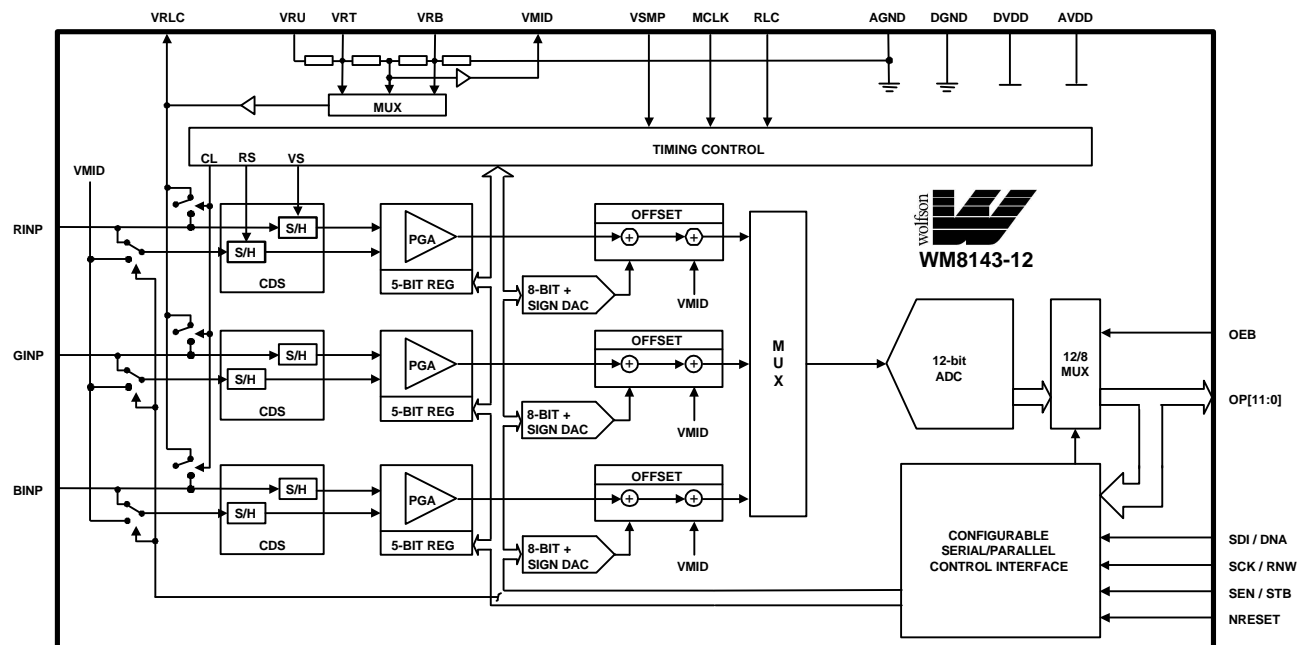
### Features

- Reset level clamp
- Correlated double sampling (CDS)
- Fine offset level shifting
- Programmable gain amplification
- 12-bit ADC with maximum 4 MSPS
- Simple clocking scheme
- Control by serial or parallel interface
- Time multiplexed eight-bit data output mode
- 32 pin TQFP package
- Interface compatible with WM8144-10 and WM8144-12

### Applications

- Flatbed scanners
- Sheet feed scanners
- Film scanners
- CCD sensor interfaces
- Contact image sensor (CIS) interfaces

### Block Diagram

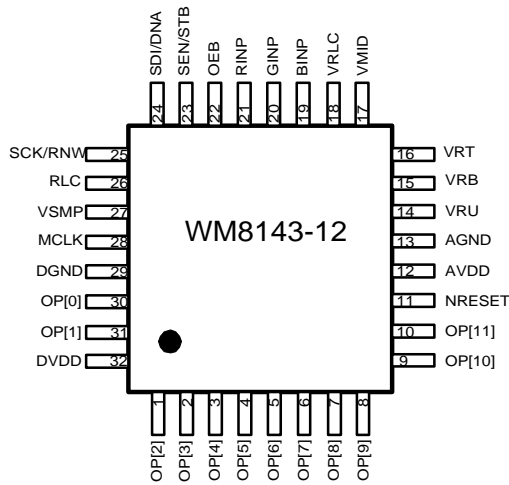


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**Pin Configuration**



**Ordering Information**

DEVICE	TEMP. RANGE	PACKAGE
WM8143-12CFT/V	0 - 70°C	32 Pin TQFP

**Absolute Maximum Ratings**

Analogue Supply Voltage ..... AGND - 0.3V, AGND +7V  
 Digital Supply Voltage ..... DGND - 0.3V, DGND +7V  
 Digital Inputs ..... DGND - 0.3V, DVDD +0.3V  
 Digital Outputs ..... DGND - 0.3V, DVDD +0.3V  
 Reference Inputs ..... AGND - 0.3V, AVDD +0.3V  
 RINP, GINP, BINP.....AGND - 0.3 V, AVDD +0.3V

Operating Temperature Range, T<sub>A</sub> ..... 0°C to +70°C  
 Storage Temperature..... -50°C to +150°C  
 Lead Temperature (10 second soldering)..... +260°C

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

**Recommended Operating Conditions**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	AVDD, DVDD		4.75		5.25	V
Operating Temperature Range	TA		0		70	°C
Input Common Mode Range	VCMR		0.5		4.5	V

## Electrical Characteristics

### Test Characteristics

AVDD = DVDD = 4.75V to 5.25V, AGND = DGND = 0V ... T<sub>A</sub> = 0°C to +70°C, MCLK = 8MHz, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current - Active				25	40	mA
Supply Current - Standby				4	10	mA
<b>Digital Inputs</b>						
High Level Input Voltage	V <sub>IH</sub>		0.8*DVDD			V
Low Level Input Voltage	V <sub>IL</sub>				0.2*DVDD	V
High Level Input Current	I <sub>IH</sub>				1	μA
Low Level Input Current	I <sub>IL</sub>				1	μA
Input Capacitance				5		pF
<b>Digital Outputs</b>						
High Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = 1mA	DVDD-0.75			V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1mA			DGND+0.75	V
High Impedance Output Current	I <sub>OZ</sub>				1	μA
<b>Input Multiplexer</b>						
CDS Mode Full Scale Input Range (V <sub>VS</sub> -V <sub>RS</sub> )		x denotes the channel selected		$\frac{2}{Gx}$		V <sub>p-p</sub>
Channel to Channel Gain Matching				1		%
Input Video Set-up Time	t <sub>VSU</sub>		10			ns
Input Video Hold Time	t <sub>VH</sub>		15			ns
Reset Video Set-up Time	t <sub>RSU</sub>	CDS Mode only	10			ns
Reset Video Hold Time	t <sub>RH</sub>	CDS Mode only	15			ns
<b>Reference String</b>						
Reference Voltage - Top	VRT	VRU = 5V	3.47	3.5	3.53	V
Reference Voltage - Bottom	VRB	VRU = 5V	1.47	1.5	1.53	V
DAC Reference Voltage	VMID	VRU = 5V	2.47	2.5	2.53	V
R.L.C. Switching Impedance				500		Ω
Reset Level Clamp Options	VRLC	VRU = 5V Voltage set by register configuration	1.46	1.5	1.54	V
			2.46	2.5	2.54	V
			3.46	3.5	3.54	V
Impedance VRT to VRB			250	500	750	Ω
Impedance VRU to AGND			1000	1500	2000	Ω
<b>8-Bit DACs</b>						
Resolution			8			Bits
Zero Code Voltage			VMID -20		VMID +20	mV

## Test Characteristics

AVDD = DVDD = 4.75V to 5.25V, AGND = DGND = 0V ... T<sub>A</sub> = 0°C to +70°C, MCLK = 8MHz, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Voltage Error			0		20	mV
Differential Non Linearity	DNL			0.1	0.5	LSB
Integral Non Linearity	INL			0.25	1	LSB
<b>12-bit ADC performance including CDS, PGA and Offset Functions NO MISSING CODES GUARANTEED</b>						
Resolution		AVDD = DVDD = 5V	12			Bits
Maximum Sampling Rate		AVDD = DVDD = 5V	4			MSPS
Zero Scale Transition Error Voltage at VINP		DAC Code = 000H, AVDD = DVDD = 5V, measured relative to VRB		± 25	±100	mV
Full Scale Transition Error Voltage at VINP		DAC Code = 000H, AVDD = DVDD = 5V, measured relative to VRT		± 25	±100	mV
Differential Non Linearity	DNL	AVDD = DVDD = 5V			+1.5	LSB
<b>PGA Gain Monotonicity Guaranteed</b>						
Red Channel Max Gain	Gr	Mode 1 AVDD = DVDD = 5V	7.5	8		Times
Green Channel Max Gain	Gg		7.5	8		Times
Blue Channel Max Gain	Gb		7.5	8		Times
<b>Switching Characteristics</b>						
MCLK Period	tPER		125			ns
MCLK High	tCKH		37.5			ns
MCLK Low	tCKL		37.5			ns
Data Set-up Time	tDSU		10			ns
Data Hold Time	tDH		10			ns
Output Propagation Delay	tPD	I <sub>OH</sub> = 1mA, I <sub>OL</sub> = 1mA			75	ns
Output Enable Time	tPZE				50	ns
Output Disable Time	tPEZ				25	ns
<b>Serial Interface</b>						
SCK Period	tSPER		125			ns
SCK High	tSCKH		37.5			ns
SCK Low	tSCKL		37.5			ns
SDI Set up Time	tSSU		10			ns
SDI Hold Time	tSH		10			ns
Set up Time - SCK to SEN	tSCE		20			ns

## Test Characteristics

AVDD = DVDD = 4.75V to 5.25V, AGND = DGND = 0V ...  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , MCLK = 8MHz, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Set up Time - SEN to SCK	tSEC		20			ns
SEN Pulse Width	tSEW		50			ns
<b>Parallel Interface</b>						
RNW Low to OP[11:4] Tri-state	tOPZ				20	ns
Address Setup Time to STB Low	tASU		0			ns
DNA Low Setup Time to STB Low	tADLS		10			ns
Strobe Low Time	tSTB		50			ns
Address Hold Time from STB High	tAH		10			ns
DNA Low Hold Time from STB High	tADLH		10			ns
Data Setup Time to STB Low	tDSU		0			ns
DNA High Setup Time to STB Low	tADHS		10			ns
Data Hold Time from STB High	tDH		10			ns
Data High Hold Time from STB High	tADHH		10			ns
RNW High to OP[11:4] Output	tOPD		0			ns

## Pin Description

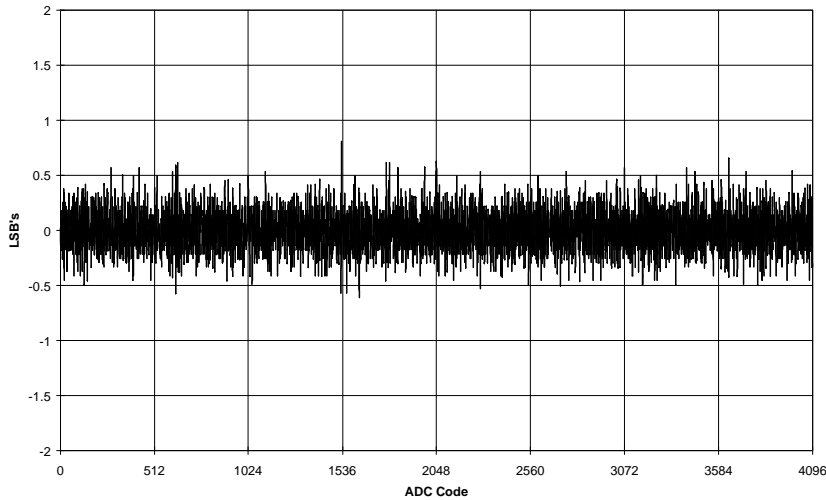
PIN	NAME	TYPE	DESCRIPTION
1	OP[2]	Digital OP	Tri-state digital 12-bit bi-directional bus. There are four modes: Tri-state: when OEB = 1 Output twelve-bit: twelve bit data is output from bus Output 8-bit multiplexed: data output on OP[11:4] at 2 * ADC conversion Rate Input 8-bit: control data is input on bits OP[11:4] in parallel mode when SCK/RNW = 0. MSB of the output word is OP[11], LSB is OP[0]
2	OP[3]	Digital OP	
3	OP[4]	Digital IO	
4	OP[5]	Digital IO	
5	OP[6]	Digital IO	
6	OP[7]	Digital IO	
7	OP[8]	Digital IO	
8	OP[9]	Digital IO	
9	OP[10]	Digital IO	
10	OP[11]	Digital IO	
11	NRESET	Digital IP	Reset input, active low. This signal forces a reset of all internal registers and selects whether the serial control bus or parallel control bus is used (see SEN/STB)
12	AVDD	Analogue supply	Positive analogue supply (5V)
13	AGND	Analogue supply	Analogue ground (0V)
14	VRU	Analogue IP	ADC reference voltages. The ADC reference range is applied between VRT (full scale) and VRB (zero level). VRU can be used to derive optimal reference voltages from an external 5V reference
15	VRB	Analogue OP	
16	VRT	Analogue OP	
17	VMID	Analogue OP	Buffered mid-point of ADC reference string
18	VRLC	Analogue OP	Selectable analogue output voltage for RLC
19	BINP	Analogue IP	Blue channel input video
20	GINP	Analogue IP	Green channel input video
21	RINP	Analogue IP	Red channel input video
22	OEB	Digital IP	Output tri-state control: all outputs enabled when OEB = 0
23	SEN/STB	Digital IP	Serial interface: enable, active high Parallel interface: strobe, active low Latched on NRESET rising edge: If low then device control is by serial interface, if high then device control is by parallel interface
24	SDI/DNA	Digital IP	Serial interface: serial interface input data signal Parallel interface: high = data, low = address
25	SCK/RNW	Digital IP	Serial interface: serial interface clock signal Parallel interface: high = OP[11:4] is output bus low = OP[11:4] is input bus
26	RLC	Digital IP	Selects whether reset level clamp is applied on a pixel-by-pixel basis. If RLC is required on each pixel then this pin can be tied high
27	VSMP	Digital IP	Video sample synchronisation pulse. This signal is applied synchronously with MLCK to specify the point in time that the input is sampled. The timing of internal multiplexing between the R, G and B channels is derived from this signal.

PIN	NAME	TYPE	DESCRIPTION
28	MCLK	Digital IP	Master clock. This clock is applied at eight, six, three or two times the input pixel rate depending on the operational mode. MCLK is divided internally to define the ADC sample rate and to provide the clock source for digital logic
29	DGND	Digital supply	Digital ground (0V)
30	OP[0]	Digital OP	See description for pins 1-10
31	OP[1]	Digital OP	See description for pins 1-10
32	DVDD	Digital supply	Positive digital supply (5V)

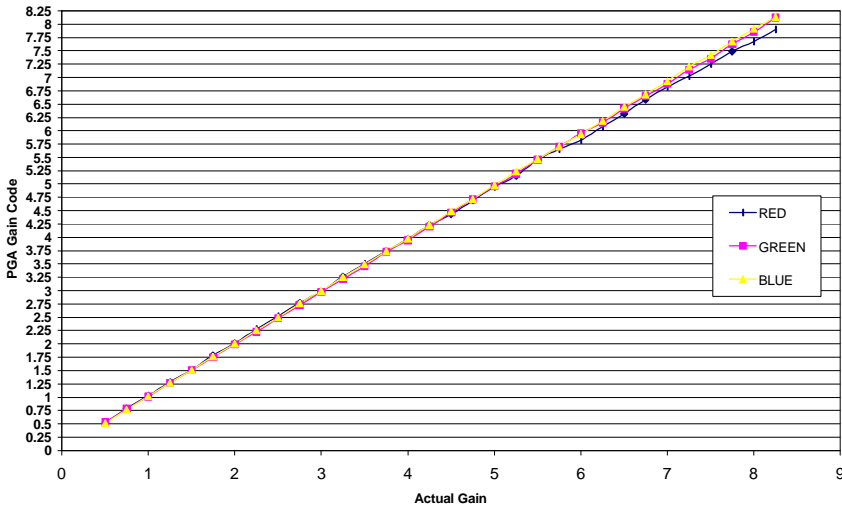
## Typical Performance

AVDD = DVDD = 5V, T<sub>A</sub> = 25°C

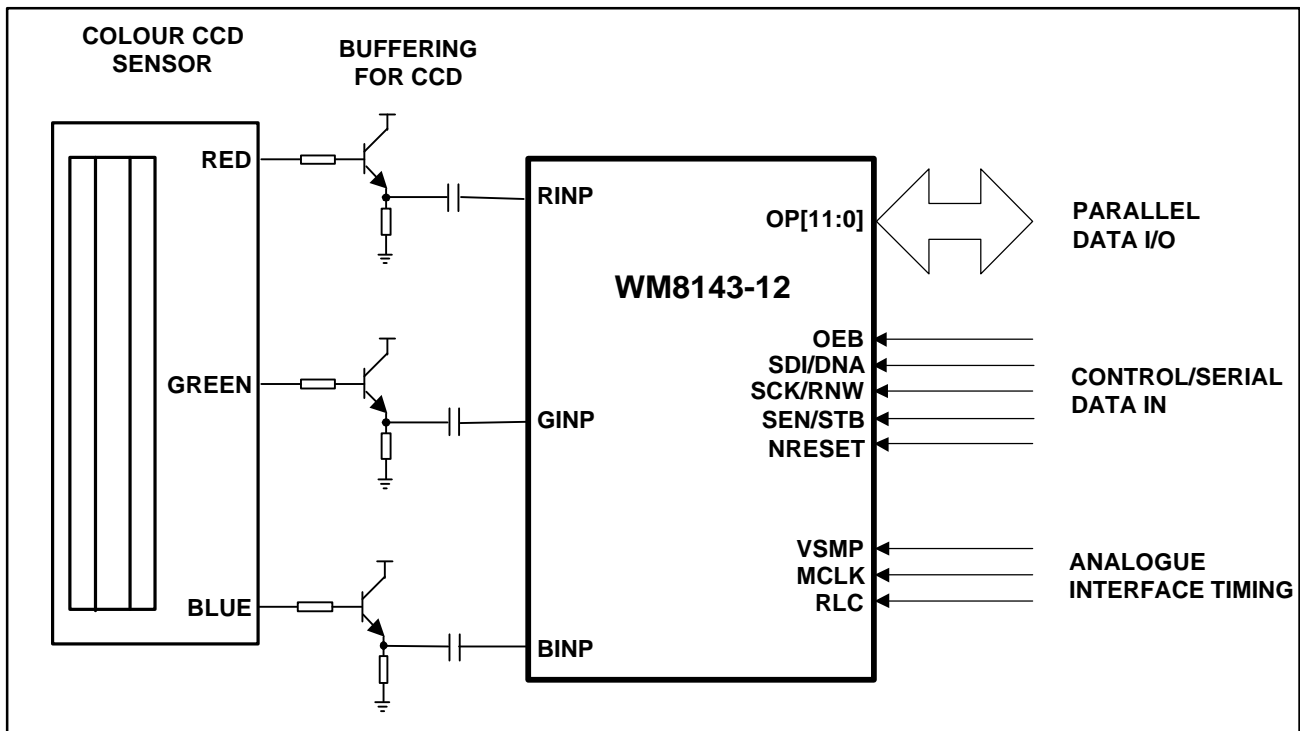
WM8143-12 DNL



PGA Gain Code vs Actual Gain



## System Description



**Figure 1 System Diagram**

The WM8143-12 signal processing IC interfaces typically via buffering and AC coupling to the output of CCD image sensors. The WM8143-12 also interfaces to CIS image sensors via DC coupling.

Analogue output signals from the image sensor are sampled, amplified and offset-corrected by the IC before being converted into digital form by an on-board high-speed 12-bit resolution analogue to digital converter. Figure 1 illustrates a typical system implementation where the three colour outputs from the CCD image sensor are buffered and AC coupled to the analogue inputs of the WM8143-12.

The digital interface to the WM8143-12 can be divided into three distinct sections: -

- **Parallel Data I/O**
- **Digital Control/Serial Timing**
- **Analogue Interface Timing**

These sections are constructed for ease of use by the system designer and are described in detail on the following pages of this datasheet.

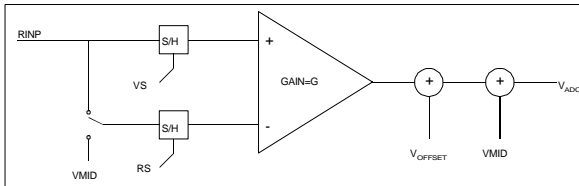


## Device Description

The WM8143-12 is configured to output 12-bit data by writing to Set-up Register 4: Bit4 (Mode12). By default the device is configured to output 10 bit data.

### S/H, Offset DACs and PGA

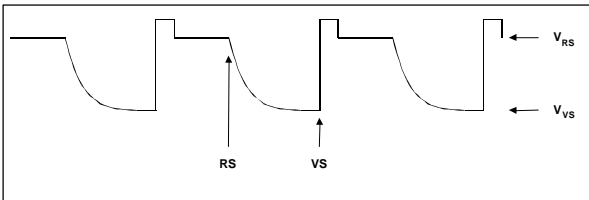
Each analogue input (RINP, GINP, BINP) of the WM8143-12 consists of a sample and hold, a programmable gain amplifier, and a DC offset correction block. The operation of the red input stage is summarised in Figure 2.



**Figure 2 Operation of Red Input Stage**

The sample/hold block can operate in two modes of operation, CDS (Correlated Double Sampling) or Single Ended.

In CDS operation the video signal processed is the difference between the voltage applied at the RINP input when RS occurs, and the voltage at the RINP input when VS occurs. This is summarised in Figure 3.



**Figure 3 Video Signal Processed in CDS Mode**

When using CDS the actual DC value of the input signal is not important, as long as the signal extremes are maintained within 0.5 volts of the chip power supplies. This is because the signal processed is the difference between the two sample voltages, with the common DC voltage being rejected.

In Single Ended operation, the VS and RS control signals occur simultaneously, and the voltage applied to the reset switch is fixed at VMID. This means that the voltage processed is the difference between the voltage applied to RINP when VS/RS occurs, and VMID. When using Single Ended operation the DC content of the video signal is not rejected.

The Programmable Gain Amplifier block multiplies the resulting input voltage by a value between 0.5 and 8.25 which can be programmed independently for each of the three input channels via the serial (or parallel) interface.

Table 1 illustrates the PGA Gains Register codes required for typical gains (see Typical Performance Graphs). The typical gain may also be calculated using the following equation:

$$\text{Typical Gain} = 0.5 + (\text{Code} * 0.25).$$

CODE	TYPICAL GAIN	CODE	TYPICAL GAIN
00000	0.5	10000	4.5
00001	0.75	10001	4.75
00010	1	10010	5.0
00011	1.25	10011	5.25
00100	1.5	10100	5.5
00101	1.75	10101	5.75
00110	2.0	10110	6.0
00111	2.25	10111	6.25
01000	2.5	11000	6.5
01001	2.75	11001	6.75
01010	3.0	11010	7.0
01011	3.25	11011	7.25
01100	3.5	11100	7.5
01101	3.75	11101	7.25
01110	4.0	11110	8.0
01111	4.25	11111	8.25

**Table 1 Typical Gain**

The DC value of the gained signal can then be trimmed by the 8 bit plus sign DAC. The voltage output by this DAC is shown as VOFFSET in Figure 2. The range of the DAC is (VMID/2) or 1.5\*(VMID/2) if the DAC\_RANGE bit in Setup Register 4 is set.

The output from the offset DAC stage is referenced to the VMID voltage. This allows the input to the ADC to maximise the dynamic range, and is shown diagrammatically in Figure 2 by the final VMID addition.

For the input stage, the final analogue voltage applied to the ADC can be expressed as:

$$V_{ADC} = G * (V_{VS} - V_{RS}) + \left[ (1 - 2 * DSIGN) * \frac{DAC\_CODE}{255} * \frac{V_{MID}}{2} \right] + V_{MID}$$

Where  $V_{ADC}$  is the voltage applied, to the ADC

$G$  is the programmed gain

$V_{VS}$  is the voltage of the video sample.

$V_{RS}$  is the voltage of the reset sample,

$DSIGN$  is the Offset DAC sign bit

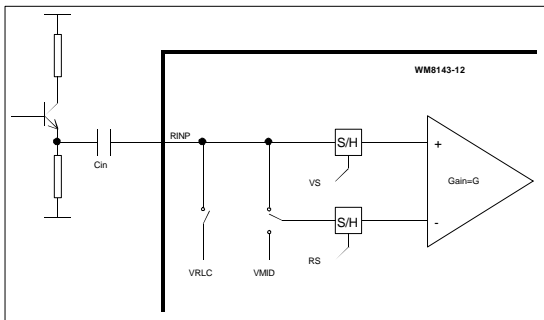
$DAC\_CODE$  is the offset DAC value.

$V_{MID}$  is the WM8143-12 generated  $V_{MID}$  voltage.

The ADC has a lower reference of  $V_{RB}$  (typically 1.5 V) and an upper reference of  $V_{RT}$  (typically 3.5 V). When an ADC input voltage is applied to the ADC equal to  $V_{RB}$  the resulting code is 000(hex). When an ADC input voltage is applied to the ADC equal to  $V_{RT}$  the resulting code is FFF(hex).

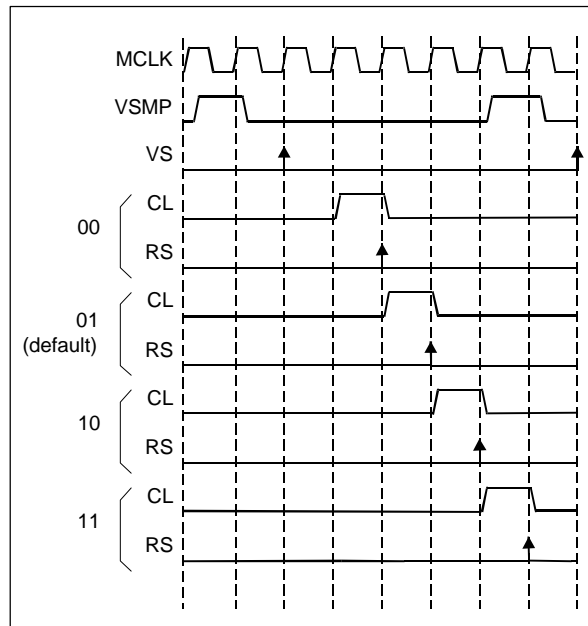
**Reset Level Clamp**

Both CDS and Single Ended operation can be used with Reset Level Clamping. A typical input configuration is shown in Figure 4.



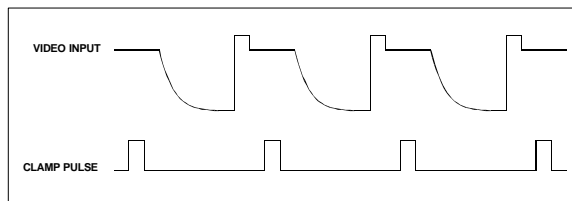
**Figure 4 Typical Input Configuration Using Reset Level Clamping**

The position of the clamp relative to the video sample is shown diagrammatically in Figure 6 and is programmable by CDSREF1-0 (see Table 6). By default, the reset sample occurs on the fourth MCLK rising edge after VSMP. The relative timing between the reset sample (and CL) and video sample can be altered as shown in Figure 5. When the clamp pulse is active the voltage on the WM8143-12 side of  $C_{in}$ , i.e. RINP, will be forced to be equal to the VRLC clamp voltage. The VRLC clamp voltage is programmable to three different levels via the serial interface. The voltage to which the clamp voltage should be programmed is dependent on the type of sampling selected and the polarity of the input video signal.



**Figure 5 Reset Sample and Clamp Timing**

For CDS operation it is important to match the clamp voltage to the amplitude and polarity of the video signal. This will allow the best use of the wide input common-mode range offered by the WM8143-12. If the input video is positive going it is advisable to clamp to VCL (Lower clamp voltage). If the video is negative going it is advisable to clamp to VCU (Upper clamp voltage). Regardless of where the video is clamped the offset DAC is programmed to move the ADC output corresponding to the reset level to an appropriate value to maximise the ADC dynamic range. For Single Ended operation it is recommended that the clamp voltage is set to VCM (middle clamp voltage).



**Figure 6 Position of Clamp Relative to Video Input**

A reset level clamp is activated if the RLC pin is high on an MCLK rising edge (Figure 7). By default this initiates an internal clamp pulse three MCLK pulses later (shown as CL in Figure 5). The relationship between CL and RS is fixed. Therefore altering the RS position also alters the CL position (Figure 5). Table 6 shows the three possible voltages to which the reset level can be clamped.

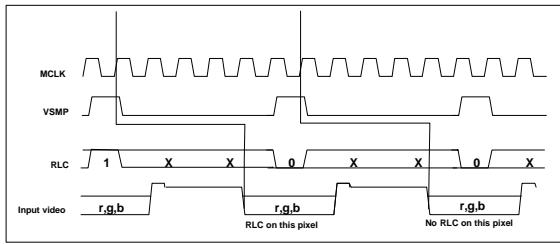


Figure 7 RLC Timing Video Sampling Options

### Video Sampling Options

The WM8143-12 can interface to CCD sensors using six basic modes of operation (summarised in Table 3). Mode configurations are controlled by a combination of control bits and timing applied to MCLK and VSMP pins. The default operational mode is mode 1: colour with CDS enabled.

#### Colour Mode Definition (Mode 1)

Figure 9 summarises the timing relationships. MCLK is applied at twice the required ADC conversion rate. Synchronisation of sampling and channel multiplexing to the incoming video signal is performed by the VSMP pulse (active high). The three input channels (R,G,B) are sampled in parallel on the rising edge of MCLK following a VSMP pulse. The sampled data is multiplexed into a single data stream at three times the VSMP rate and passes through the internal pipeline and emerges on the OP[11:0] bus. Both Correlated Double Sampling (CDS) and Single Ended modes of operation are available.

#### Monochrome Mode Definitions

One input channel is continuously sampled on the rising edge of MCLK following a VSMP pulse. The user can specify which input channel (R,G,B) is to be sampled by writing to the WM8143-12 internal control registers. There are four separate monochrome modes with different maximum sample rates and CDS availability.

#### Monochrome Mode (Mode 2)

Figure 10 summarises the timing relationships. The timing in this mode is identical to mode 1 except that one input channel is sampled three times (due to the multiplexer being held in one position) and passes through the device as three separate samples. The last two samples can be ignored at the output OP[11:0].

#### Fast Monochrome Mode (Mode 3)

Figure 11 summarises the timing relationships. This mode allows the maximum sample rate to be increased to 2.67 MSPS. This is achieved by altering the MCLK:VSMP ratio to 3:1. In this mode, the timing of RS and CL must be fixed (refer to Table 3). The sampled video data will pass through the internal pipeline and emerge on the OP[11:0] bus.

#### Max. Speed Monochrome Mode (Mode 4)

Figure 12 summarises the timing relationships. This mode allows the maximum sample rate to be increased to 4 MSPS. This is achieved by altering the MCLK:VSMP ratio to 2:1. The latency through the device is identical to modes 1 and 2. CDS is not available in this mode.

#### Slow Colour Mode (Mode 5)

Figure 13 summarises the timing relationships. This mode is identical to Mode 1 except that the MCLK to VSMP ratio is 8 : 1 and the maximum sample rate is 1 MSPS. To obtain a ratio of 4:4 between the video sample position and the reset sample position, Setup Register 3 CDSREF1-0 control bits b[5:4] should be set to 10. The first three of the four output words are valid.

#### Slow Monochrome Mode (Mode 6)

Figure 14 summarises the timing relationships. This mode is identical to mode 2 except that the MCLK to VSMP ratio is 8 : 1 and the maximum sample rate is 1 MSPS. To obtain a ratio of 4:4 between the video sample position and the reset sample position, Setup Register 3 CDSREF 1-0 control bits b[5:4] should be set to 10. The first of the four output words is the only valid output.

### Input Impedance

The input impedance of the WM8143-12 is dependent upon the sampling frequency of the input signal and the gain that the PGA is set to. This is due to the effective capacitance of the 'sample and hold' circuits (Figure 8).

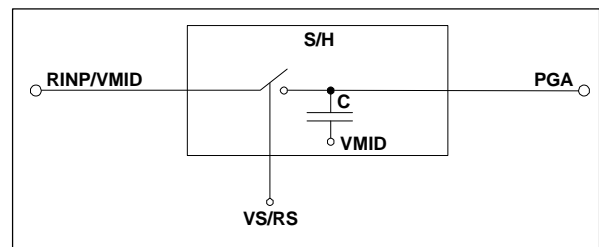


Figure 8 Input Impedance S/H Circuit

When the VS/RS control is activated the switch closes and the effective impedance of the input is  $1/CF$  where the value of C changes from 0.3pF for minimum gain to 9.6pF for maximum gain and F is the sample frequency in Hz. Table 2 illustrates the maximum and minimum input impedance at different frequencies.

<b>SAMPLING FREQUENCY (MHz)</b>	<b>IMPEDANCE (M<math>\Omega</math>) MIN GAIN</b>	<b>IMPEDANCE (K<math>\Omega</math>) MAX GAIN</b>
0.5	6.6	208
1	3.3	104
2	1.6	52
4	0.8	26

**Table 2 Effects of Frequency on Input Impedance**

## Calibration

To achieve optimum performance of the WM8143-12, a calibration procedure must be implemented. This is achieved by using a combination of the gain and offset functions to amplify and shift the input signal so that it lies within and maximises the input ADC range.

MODE	DESCRIPTION	CDS AVAIL-ABLE	MAX. SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIRE-MENTS	REGISTER CONTENTS WITH CDS	REGISTER CONTENTS WITHOUT CDS*
1	Colour	Yes	1.33MSPS	Three input channels (R, G, B) are sampled in parallel at max. 1.33MSPS. The sampled data is multiplexed into a single data stream before the internal ADC, giving an internal serial rate of max. 4MSPS	MCLK max. 8MHz. MCLK: VSMP ratio is 6:1	Setup Reg. 1: 03(H)	Setup Reg. 1: 01(H)
2	Monochrome	Yes	1.33MSPS	One input channel is continuously sampled. The internal multiplexer is held in one position under control of the user.	Identical to Mode 1	Setup Reg. 1: 07(H) Setup Reg. 3: bits b[7-6] define which channel is sampled	Setup Reg. 1: 05(H) Setup Reg. 3: bits b[7-6] define which channel is sampled
3	Fast Monochrome	Yes	2.67MSPS	Identical to Mode 2 except that max. sample rate is 2.67MSPS	MCLK max. 8MHz. MCLK: VSMP ratio is 3:1	Identical to Mode 2 plus Setup Reg. 3: bits b[5-4] must be set to 00(H)	Identical to Mode 2
4	Max. Speed Monochrome	No	4MSPS	Identical to Mode 2 except that max. sample rate is 4MSPS	MCLK max. 8MHz. MCLK: VSMP ratio is 2:1	Not applicable	Setup Reg. 1: 45(H) Setup Reg. 3: bits b[7-6] define which channel is sampled
5	Slow Colour	Yes	1MSPS	Identical to Mode 1 except that max. sample rate is 1MSPS	MCLK max. 8MHz. MCLK: VSMP ratio is 8:1	Identical to Mode 1	Identical to Mode 1
6	Slow Monochrome	Yes	1MSPS	Identical to Mode 2 except that max. sample rate is 1MSPS	MCLK max. 8MHz. MCLK: VSMP ratio is 8:1	Identical to Mode 2	Identical to Mode 2

\* Only indicates relevant register bits

**Table 3 WM8143-12 Mode Summary**

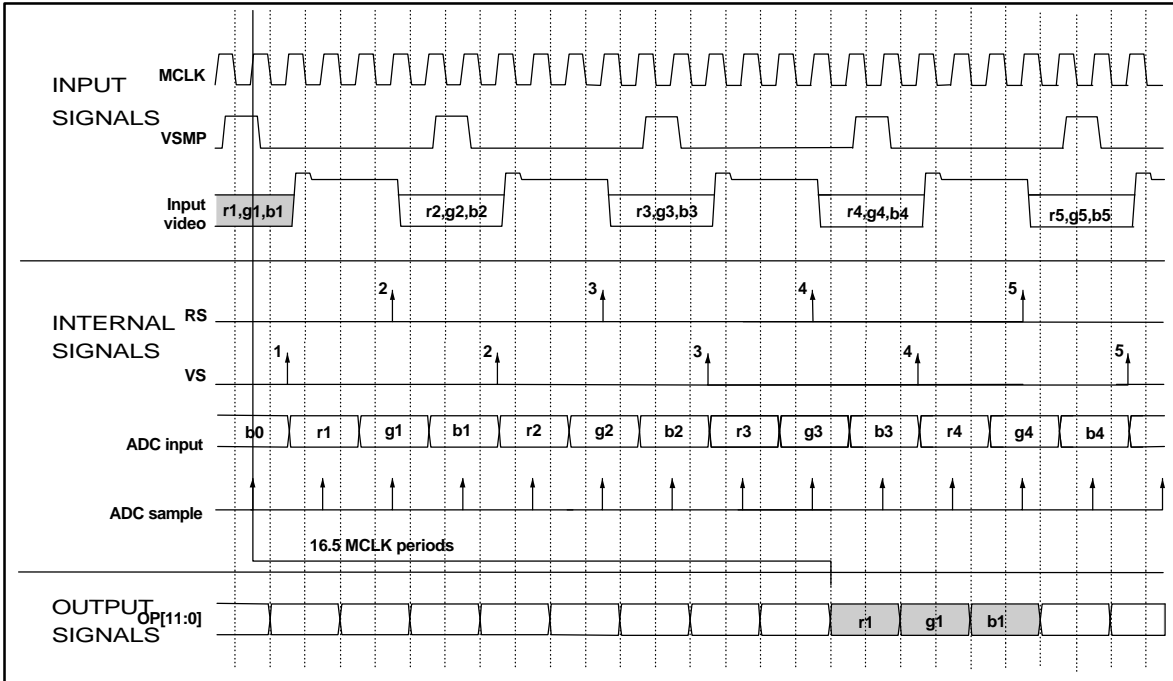


Figure 9 Default Timing in CDS Colour Mode (Mode 1)

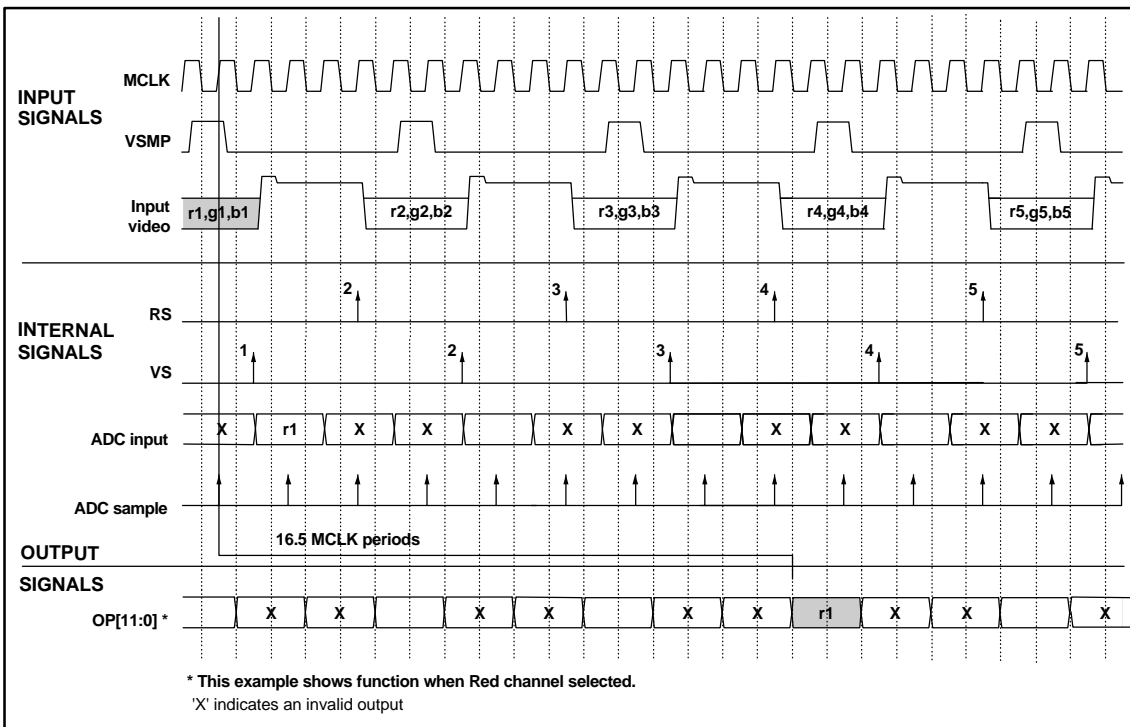


Figure 10 Default Timing in CDS Monochrome Mode (Mode 2)

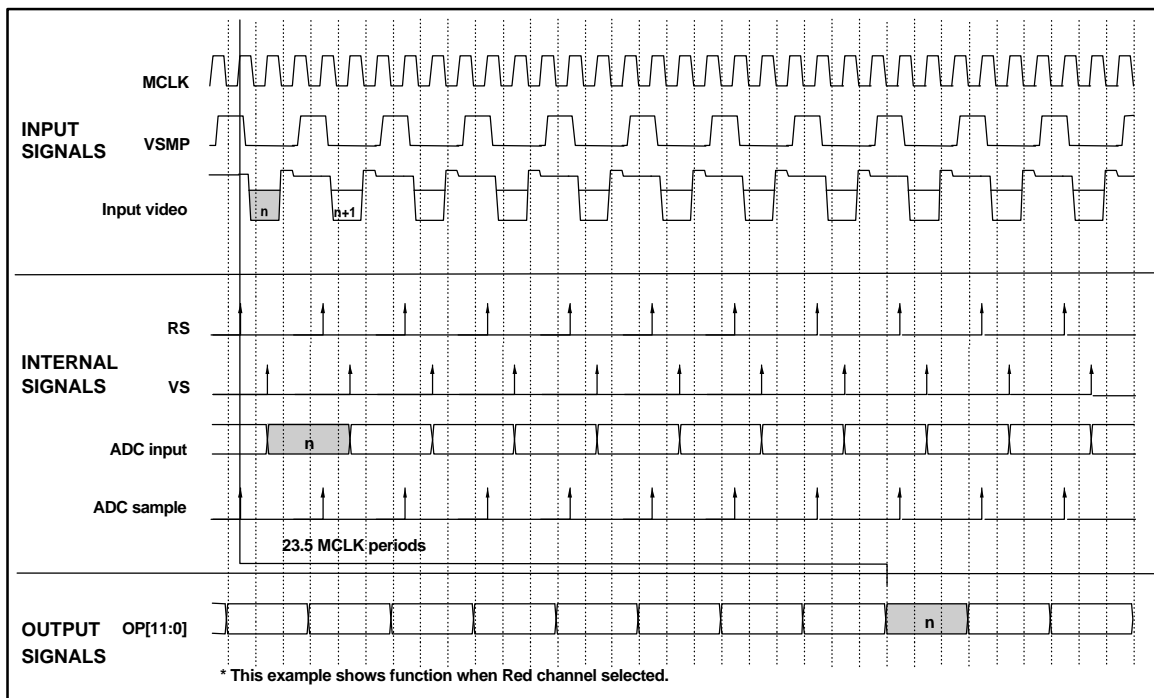


Figure 11 Default Timing in Fast CDS Monochrome Mode (Mode 3)

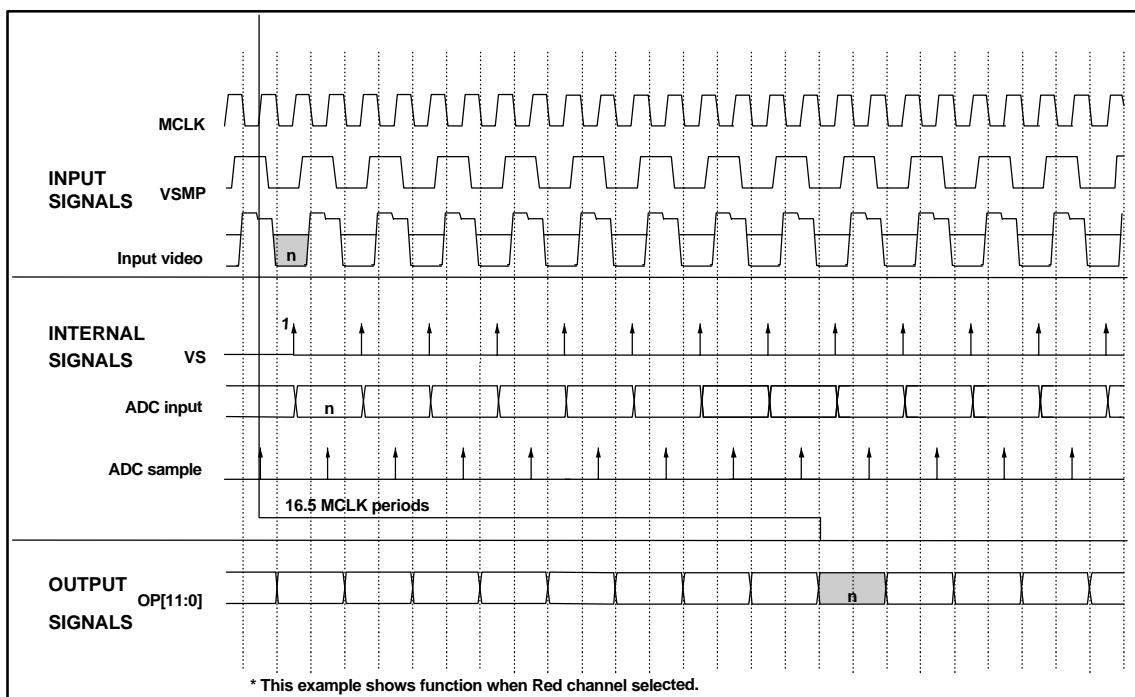


Figure 12 Default Timing in Max. Speed non-CDS Monochrome Mode (Mode 4)

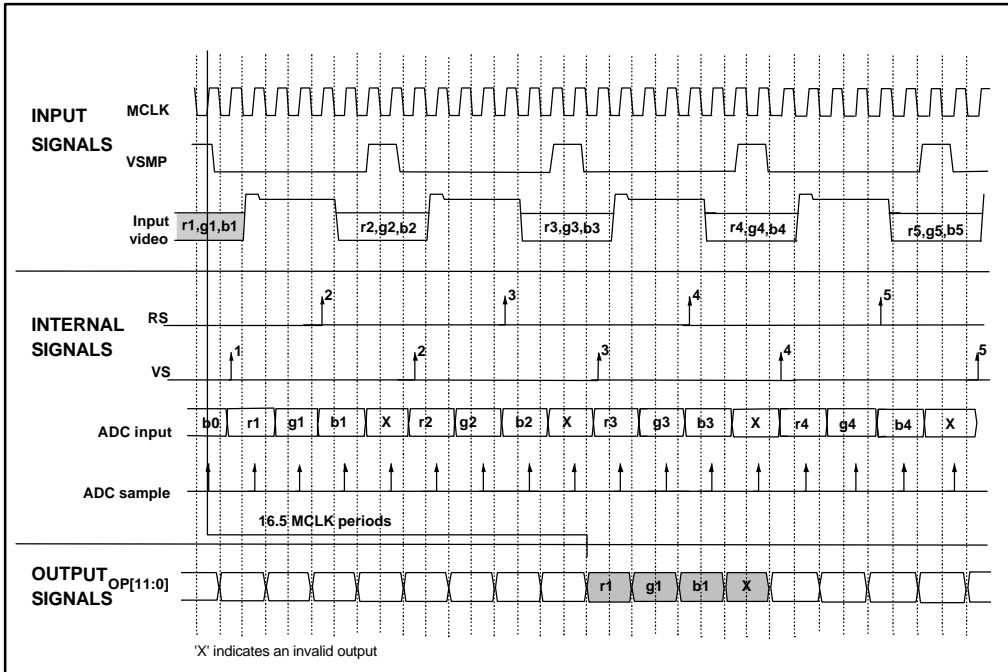


Figure 13 Default Timing in Slow CDS Colour Mode (Mode 5)

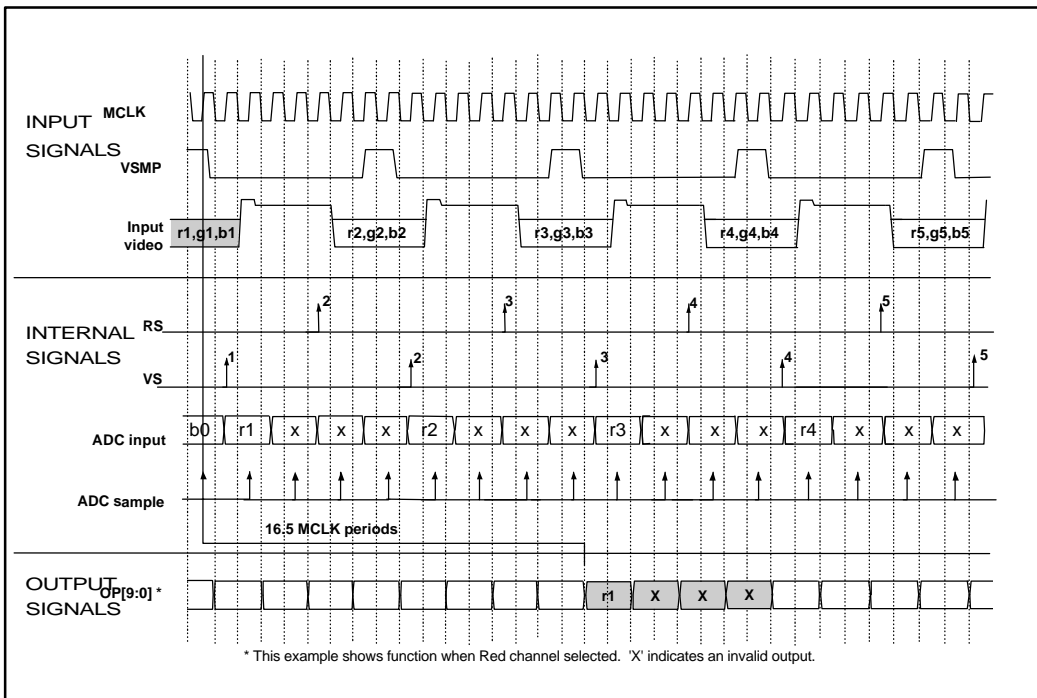


Figure 14 Default timing in Slow CDS Monochrome Mode (Mode 6)

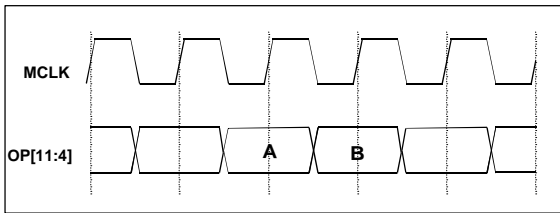


## Applications Recommendations

### Output Data Interface

By default, data is output from the device as a twelve-bit wide word on OP[11:0]. Optionally, data can be output in an eight-bit word format. Figure 15 shows this function. Data is presented on pins OP[11:4] at twice pixel rate.

In mode 3, the output is spread over three MCLK periods. The first two periods contain byte A data and the third period has byte B data. Either of the two byte A data periods are valid.



**Figure 15 Eight-bit Multiplexed Bus Output**

- Ad11,d10,d9,d8,d7,d6,d5,d4 - First byte
- Bd3,d2,d1,d0,PNS,CC1,CC0,ORNG - Second byte
- PNS: This bit shows if the device is configured in parallel or serial mode. 1 = Parallel, 0 = Serial.
- CC1/CC0: These bits show which channel the current output was taken from. 00 = RED, 01 = GREEN, 10 = BLUE.
- ORNG: This bit indicates if the current output pixel has exceeded the maximum or minimum range during processing. 1 = out of range, 0 = within range.

### Control Interface Selection

WM8143-12 can be controlled via a serial or parallel interface. The decision on which interface is to be used is made on the sense of the SEN/STB pin on the rising edge of the NRESET signal.

SEN/STB	CONDITION	MODE
0	NRESET rising edge	Serial Interface
1	NRESET rising edge	Parallel Interface

**Table 4 WM8143-12 Interface Set-up**

It is expected that this would be achieved on system power-up by attaching a simple RC network to the NRESET pin. The RC network should delay the set up

on the NRESET pin until the other conditions have been established. This feature is only activated on a hardware reset (using the NRESET pin). The software reset does not sample SEN/STB.

### Controlling the WM8143-12

The WM8143-12 can be configured through a serial interface or a parallel interface. Selection of the interface type is by the SEN/STB pin which must be tied high (parallel) or low (serial) as shown in Table 4.

#### Serial Interface

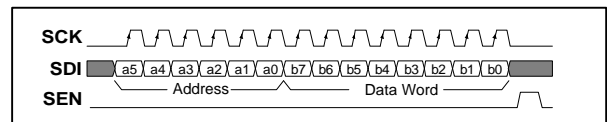
The serial interface consists of three pins (refer to Figure 16). A six-bit address is clocked in MSB first followed by an eight-bit data word, also MSB first. Each bit is latched on the rising edge of SCK. Once the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register.

#### Parallel Interface

The parallel interface uses bits [11:4] of the OP bus as well as the STB, DNA and RNW pins (refer to Figure 17). Pin RNW must be low during a write operation. The DNA pin defines whether the data byte is address (low) or data (high). The data bus OP[11:4] is latched in during the low period of STB.

### Internal Register Definition

Table 5 summarises the internal register content. The first 5 addresses in the table are used to program setup registers and to provide a software reset feature ( 00H is reserved). The remaining 3 entries in the table define the address location of internal data registers. In each case, a further three sub-addresses are defined for the red, green and blue register. Selection between the red, green and blue registers is performed by address bits a1 and a0, as defined in the table. Setting both a1 and a0 equal to 1 forces all three registers to be updated to the same data value. Blank entries in Table 5 should be programmed to zero.



**Figure 16 Serial Interface Timing**

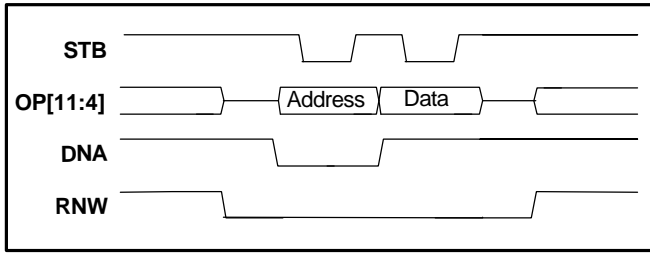


Figure 17 Parallel Interface Timing

ADDRESS <a5:a0>	DES- CRIPTION	DE- FAULT (HEX)	BIT							
			b7	b6	b5	b4	b3	b2	b1	b0
000000	Reserved									
000001	Setup Register 1	03		VSMP4M				MONO	CDS	ENADC
000010	Setup Register 2	00						INVOP		MUXOP
000011	Setup Register 3	11	CHAN[1]	CHAN[0]	CDSREF[1]	CDSREF[0]			RLC[1]	RLC[0]
000100	Software Reset	00								
000101	Setup Register 4	00				MODE 12			DACRNG	
1000a1a0	DAC Values	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
1001a1a0	DAC Signs	00								DSIGN
1010a1a0	PGA Gains	00				PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]

ADDRESS LSB DECODE	a1	a0
Red Register	0	0
Green Register	0	1
Blue Register	1	0
Red, Green and Blue	1	1

Table 5 Register Map Contents

REGISTER	BIT NO	BIT NAMES(S)	DEFAULT	DESCRIPTION
Setup Register 1 Address ,<a5:a0> 000001	0	ENADC	1	ADC Standby Control: 0 = Standby, 1 = Active
	1	CDS	1	Correlated Double Sampling Mode: 0 = Single Ended Mode, 1 = CDS Mode
	2	MONO	0	Mono/Colour Select: 0 = Colour, 1 = Monochrome Operation
	6	VSMP4M	0	Required when operating in Mode 4: 0 = Other Modes, 1 = Mode 4
Setup Register 2 Address ,<a5:a0> 000010	0	MUXOP	0	Eight Bit Output Mode: 0 = 12-bit, 1 = 8-bit Multiplexed
	2	INVOP	0	Inverts ADC Output: 0 = Non-inverting, 1 = Inverting
Setup Register 3 Address ,<a5:a0> 000011	1-0	RLC1-0	01	Reset Level Clamp Voltage: 00 = 1.5V 01 = 2.5V 10 = 3.5V 11 = Reserved
	5-4	CDSREF1-0	01	CDS Mode Reset Timing Adjust: 00 = Advance 1 MCLK Period 01 = Normal 10 = Retard 1 MCLK Period 11 = Retard 2 MCLK Periods
	7-6	CHAN1-0	00	Monochrome Mode Channel Select: 00 = Red channel 01 = Green channel 10 = Blue channel 11 = Reserved
Setup Register 4 Address ,<a5:a0> 000101	1	DACRNG	0	Offset DAC Output Range: 0 = DAC Output Range = $V_{mid}/2 = +/-1.25V$ 1 = DAC Output Range = $1.5 * (V_{mid}/2) = +/-1.875V$
	4	MODE 12	0	Enable 12-bit ADC Output: 0 = 10 bit, 1 = 12 bit

Table 6 Control Bit Descriptions

Detailed Timing Diagrams

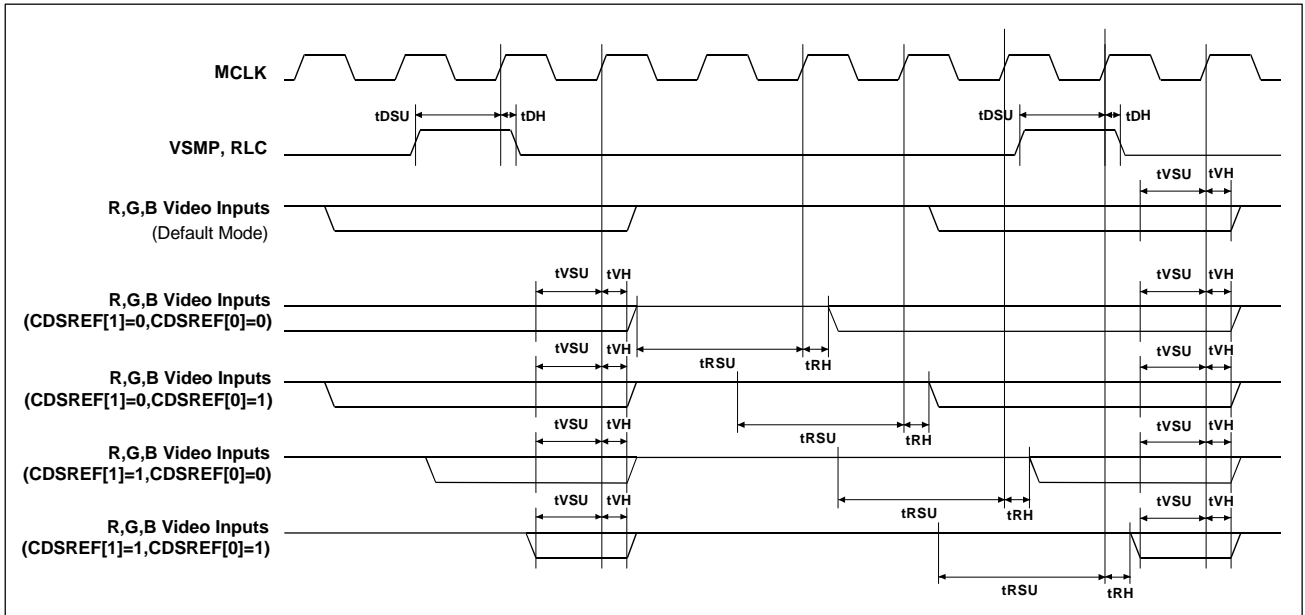


Figure 18 Detailed Video Input Timing - Modes 1 and 2

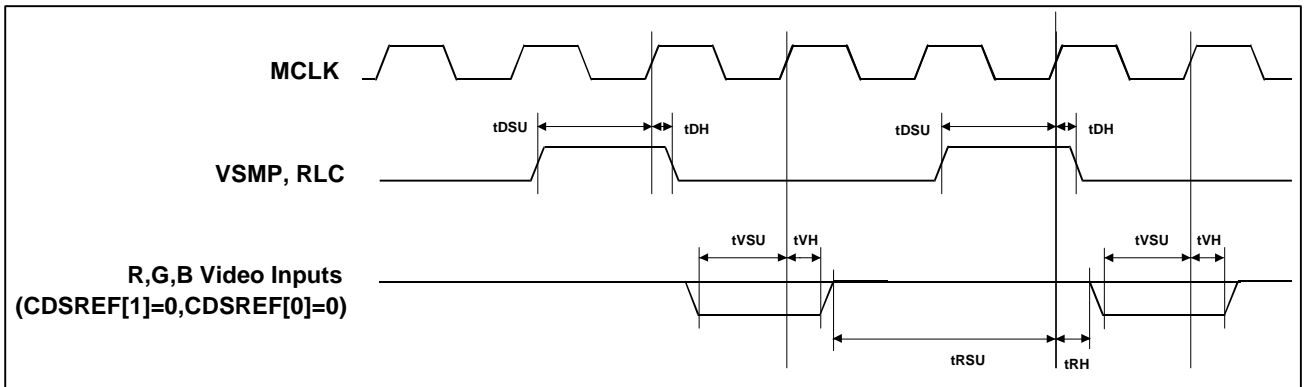


Figure 19 Detailed Video Input Timing - Mode 3

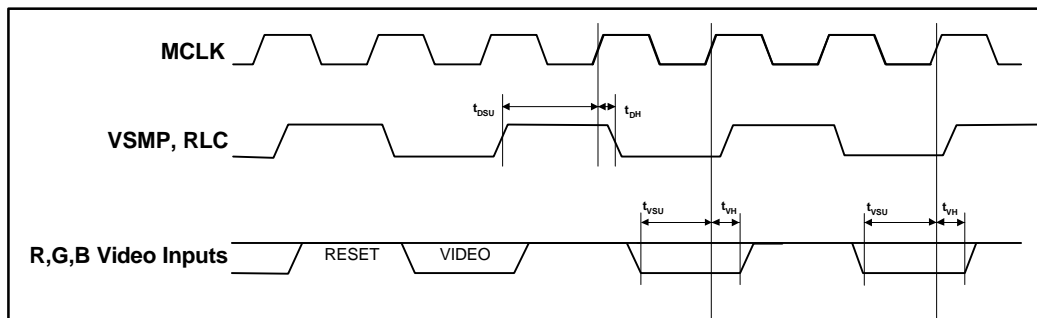


Figure 20 Detailed Video Input Timing - Mode 4

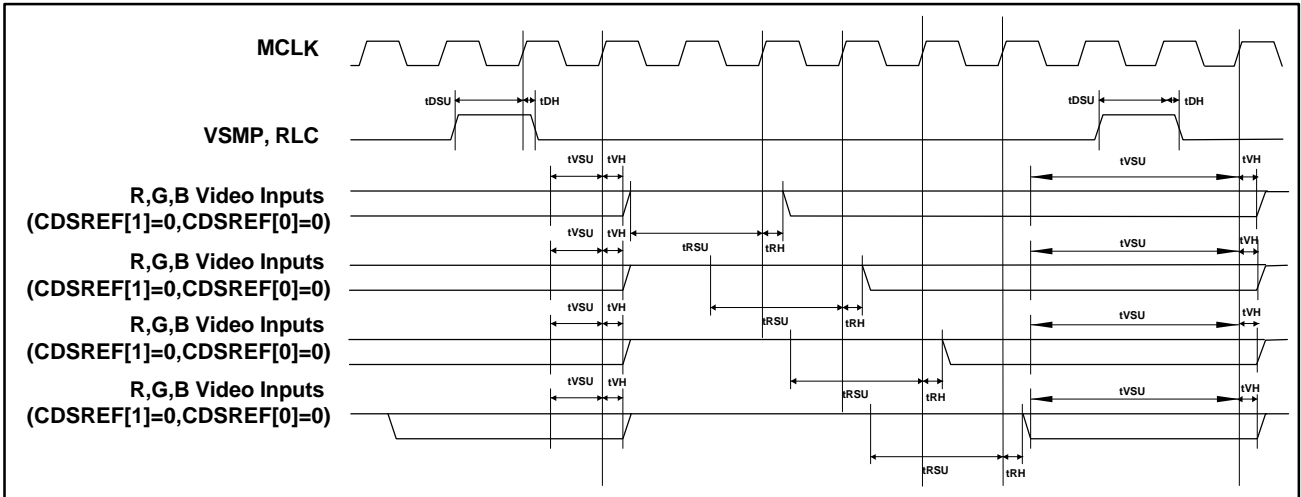


Figure 21 Detailed Video Timing - Modes 5 and 6

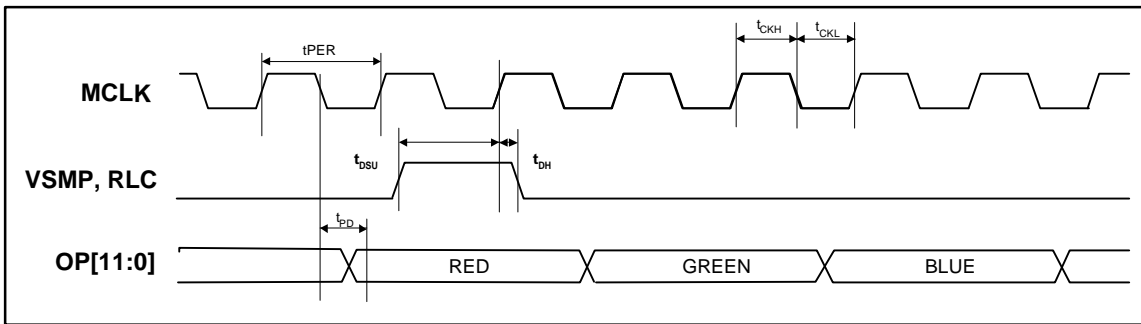


Figure 22 Detailed Digital Timing - Modes 1 and 2

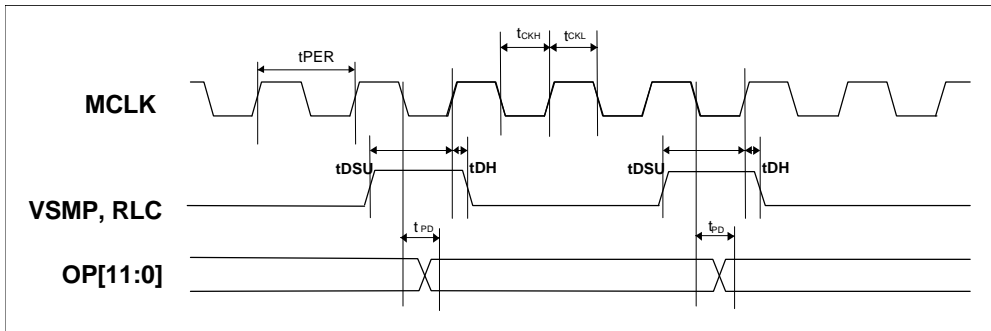


Figure 23 Detailed Digital Timing – Mode 3

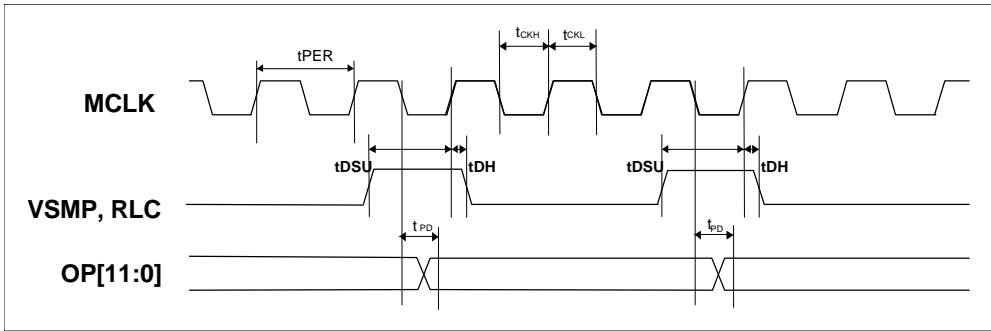


Figure 24 Detailed Digital Timing – Mode 4

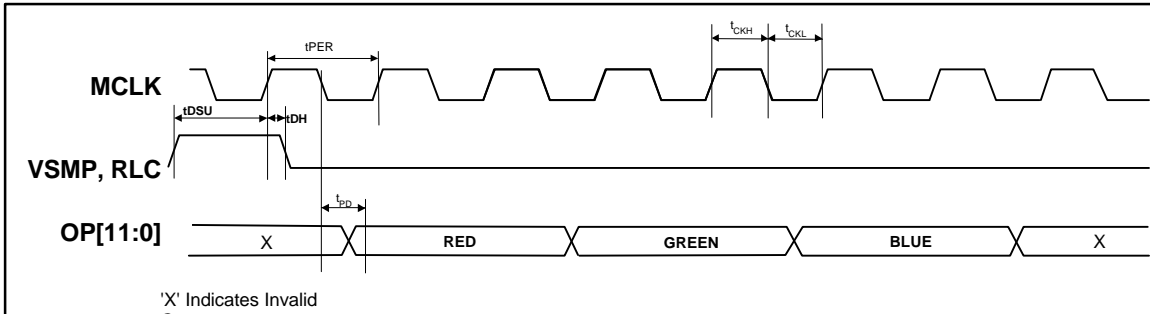


Figure 25 Detailed Digital Timing – Modes 5 and 6

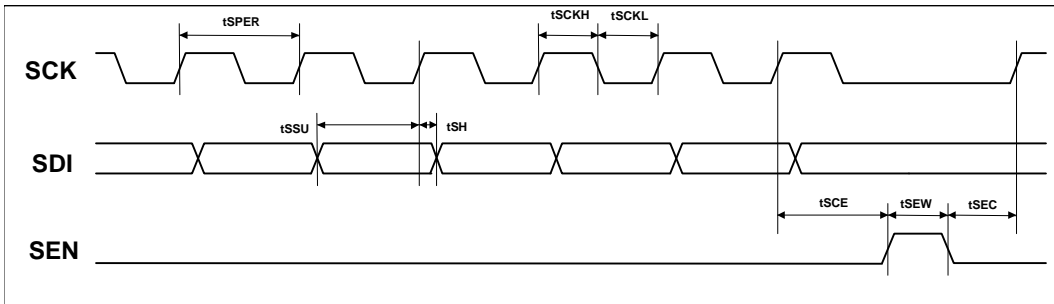


Figure 26 Detailed Timing Diagram for Serial Interface

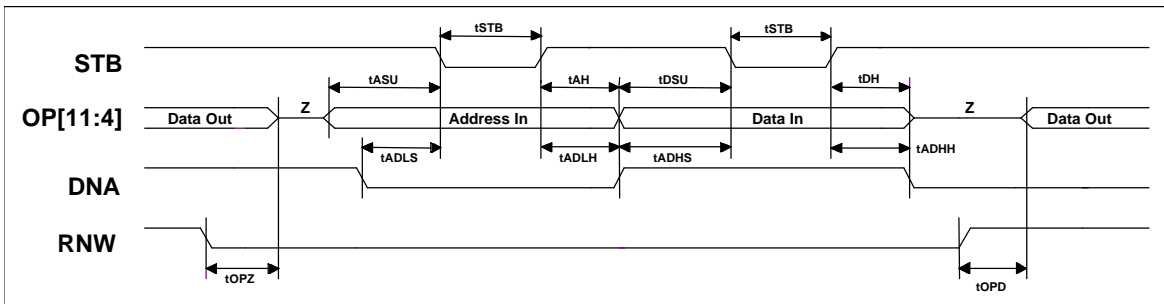
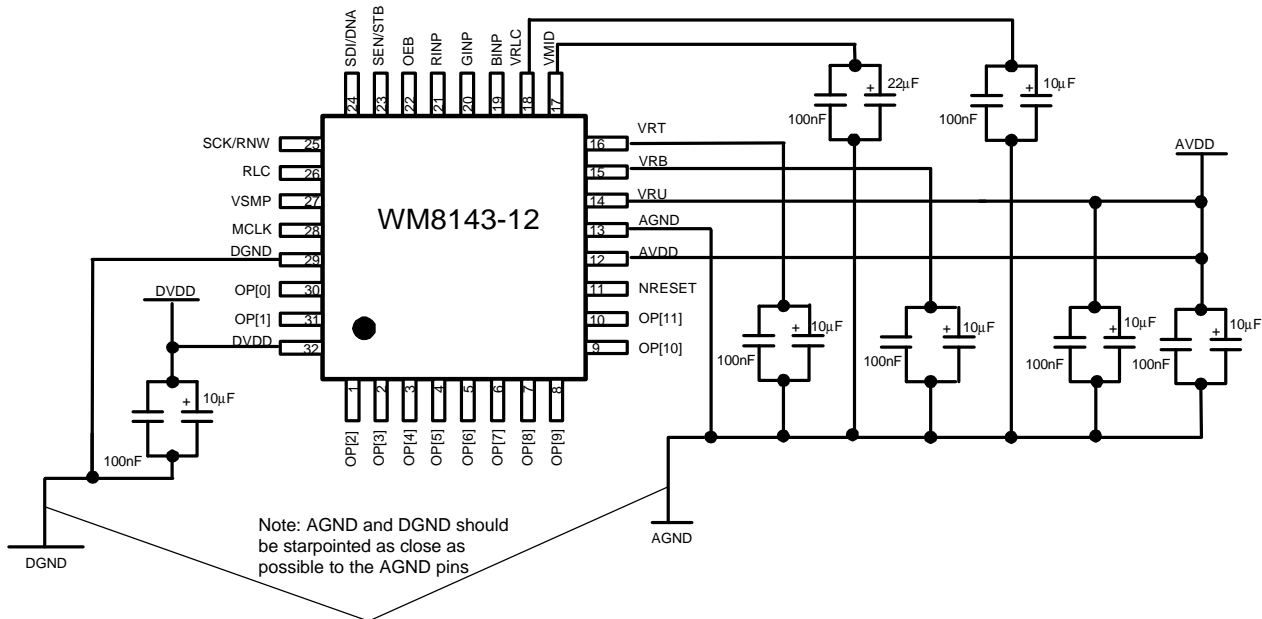
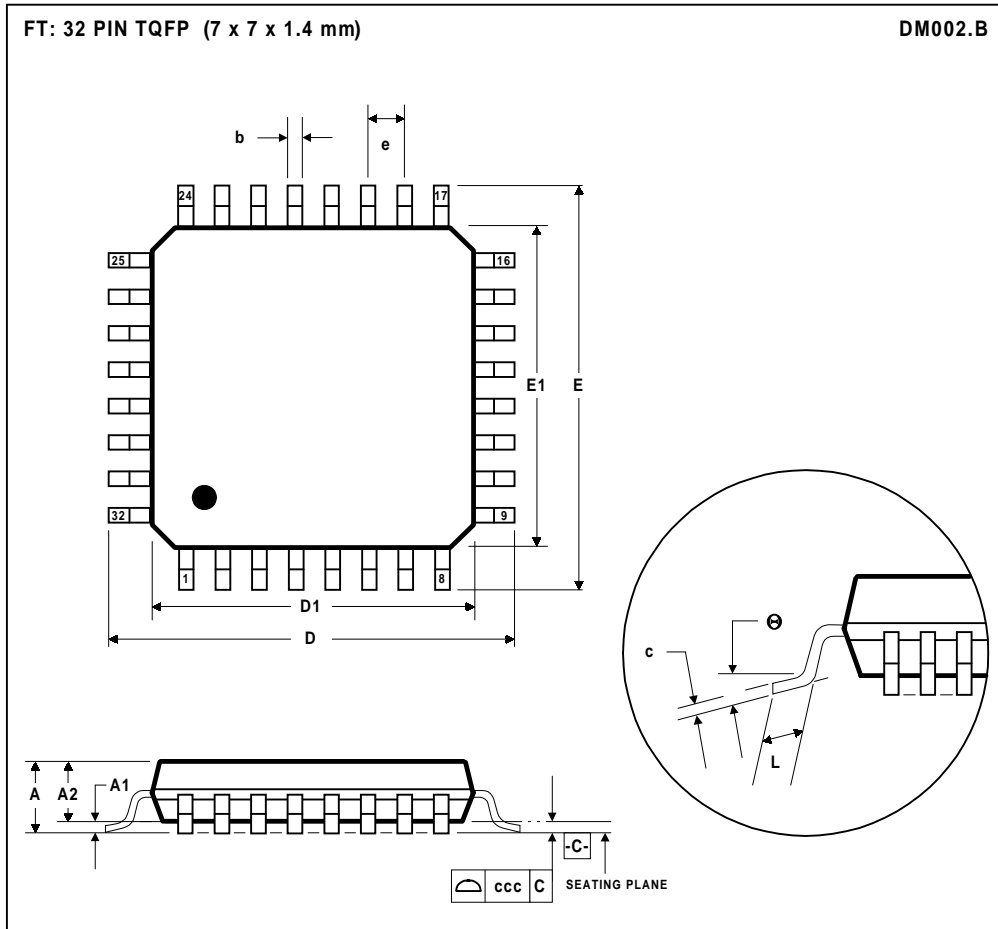


Figure 27 Detailed Timing Diagram for Parallel Interface

# Applications Diagram



Package Dimensions



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
<b>A</b>	-----	-----	1.60
<b>A<sub>1</sub></b>	0.05	-----	0.15
<b>A<sub>2</sub></b>	1.35	1.40	1.45
<b>b</b>	0.30	0.37	0.45
<b>c</b>	0.09	-----	0.20
<b>D</b>	9.00 BSC		
<b>D<sub>1</sub></b>	7.00 BSC		
<b>E</b>	9.00 BSC		
<b>E<sub>1</sub></b>	7.00 BSC		
<b>e</b>	0.80 BSC		
<b>L</b>	0.45	0.60	0.75
<b>θ</b>	0°	3.5°	7°
Tolerances of Form and Position			
<b>ccc</b>	0.10		
<b>REF:</b>	JEDEC.95, MS-026		

NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.  
 D. MEETS JEDEC.95 MS-026, VARIATION = BBA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

Last page of WM8143-12 Datasheet