The "Interworking Element for 8 E1/T1 lines" (IWE8), PXB 4220 and PXB 4221 are members of Infineon" ATM Chipset. Together with framing and line interface components (e.g. Infineon's QuadFALC PEB 22554) the IWE8 serves as gateway between Asynchronous Transfer Mode (ATM) networks and timeslot based PDH networks.

The IWE8 is a single chip multiservice device that integrates ATM cell handling and TDM circuit to ATM cell interworking in E1/T1 applications. Each of the 8 E1 or T1 input and output ports can be configured independently to operate in ATM Mode or AAL Mode. It is a very flexible solution supporting multiple services with a minimum of devices.

IWE8

Features

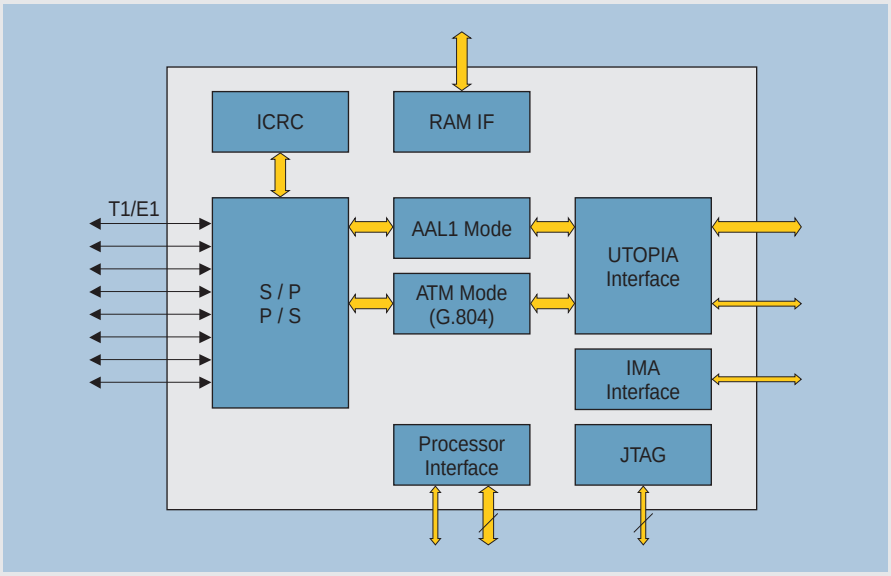
- Full duplex ATM Packetizer/ Depacketizer for 8 E1/T1 highways
- Configurable to T1 or E1 mode via external pin
- 8 T1/E1 ports configurable independently to ATM or AAL Mode
- ATM Mode:
  - ATM cell mapping into PDH according to ITU-T G.804
  - B-ISDN User-Network Interface
  - Physical Layer Operation at 1544 kbit/s and 2048 kbit/s according to ITU-T I.432.3
- AAL Mode (PXB 4220/4221):
  - AAL1 according to ITU-T I.363.1 or transparent without any adaptation layer overhead (AAL0)
  - Structured T1/E1 N x 64 kbit/s service
  - Channel Associated Signalling (CAS)
  - Partially filled cells with programmable filling thresholds
  - Reassembly buffer can compensate up to +/- 4 ms Cell Delay Variation (CDV)
  - Statistics counters per channel for lost/misinserted/errored cells etc.
  - Internal clock recovery circuit using Synchronous Residual Time Stamp (SRTS) or Adaptive Clock Method (ACM) for unstructured CES ports. Optionally, it's possible to order the PXB 4221 device, which comes without SRTS clock recovery.
- Inverse Multiplexing over ATM (IMA) interface
- 8 generic framer interfaces with integrated transmit clock selector supporting
  - Synchronous Mode (SYM)
  - Generic Interface Mode (GIM)
  - FALC Mode (FAM): Glue-less interface for Infineon's Framer and Line Interface Components (FALC)
  - Echo Canceller Mode (EC): ATM cells are duplicated internally and transmitted via two framer ports
- UTOPIA industry standard interface:
  - Level 2 in slave mode; 8 data, 5 address lines
  - Level 1 in master/slave mode
  - UTOPIA clock up to 38.88 MHz

IWE8
PXB 4220/4221

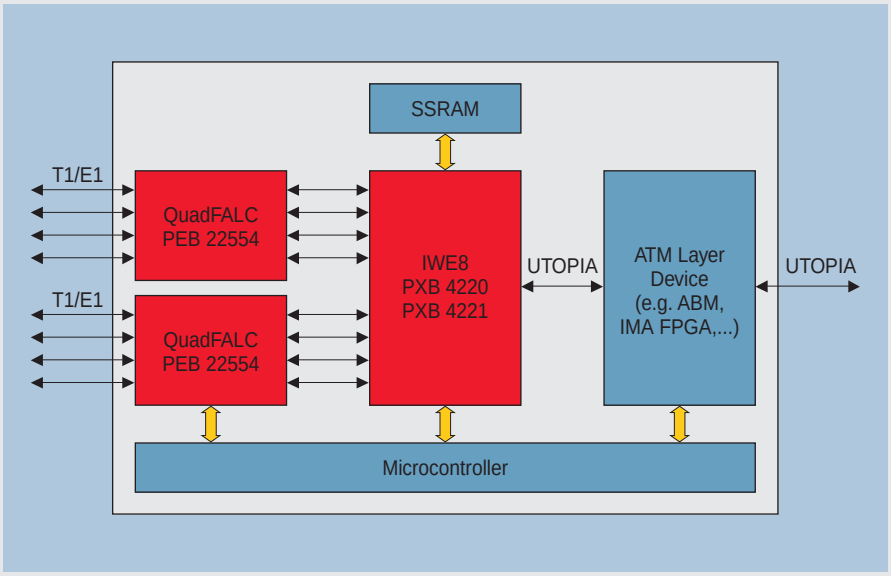
Infineon technologies

Never stop thinking.

- 16-Bit generic microprocessor interface for control and configuration of the chip runs either in Intel 386EX or Motorola compatible mode
- External synchronous Flow-Through SSRAM 1 x 64 K x 33 Bit or 1 x 64 K x 32 Bit required
- Build-in data path loops for test
- Cell insertion/extraction via microprocessor interface
- 3.3 V power supply with 5 V tolerant inputs
- Typical power dissipation 1 W
- P-BGA 256 package
- Temperature range from -40° to +85°C



PXB 4220/PXB 4221 Networking Element for 8 T1/E1 Ports (IWE8)



PXB 4220/PXB 4221 Application Example: Line Interface Card

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