CY29352

2.5V or 3.3V, 200-MHz, 11-Output Zero Delay Buffer

Features

- **Output frequency range: 16.67 MHz to 200 MHz**
- **Input frequency range: 16.67 MHz to 200 MHz**
- **2.5V or 3.3V operation**
- **Split 2.5V/3.3V outputs**
- **±2% max Output duty cycle variation**
- **11 Clock outputs: Drive up to 22 clock lines**
- **LVCMOS reference clock input**
- **125-ps max output-output skew**
- **PLL bypass mode**
- **Spread Aware™**
- **Output enable/disable**
- **Pin compatible with MPC9352 and MPC952**
- **Industrial temperature range: –40°C to +85°C**
- **32-Pin 1.0mm TQFP package**

Description

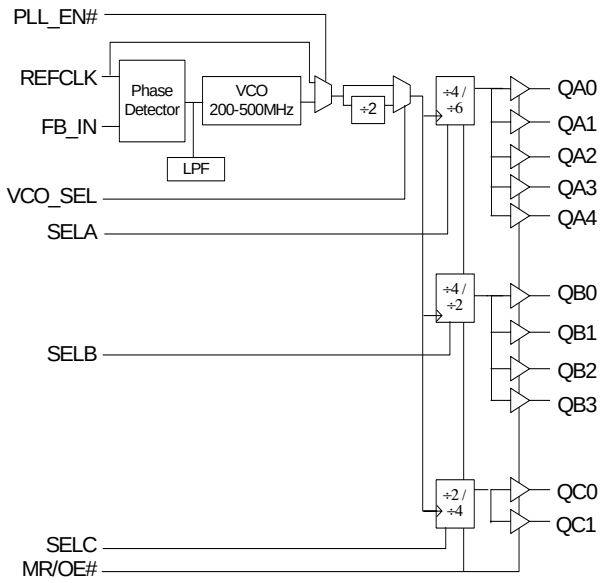
The CY29352 is a low voltage high performance 200-MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

The CY29352 features an LVCMOS reference clock input and provides 11 outputs partitioned in 3 banks of 5, 4, and 2 outputs. Bank A divides the VCO output by 4 or 6 while Bank B divides by 4 and 2 and Bank C divides by 2 and 4 per SEL(A:C) settings, see *Function Table*. These dividers allow output to input ratios of 3:1, 2:1, 3:2, 1:1, 2:3, 1:2, and 1:3. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:22.

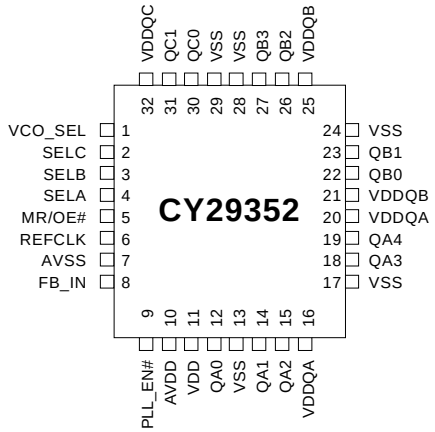
The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 16.67 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see *Table 1.*

When PLL_EN# is HIGH, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	I/O	Type	Description
6	REFCLK	I, PD	LVCMOS	**Reference clock input**.
12, 14, 15, 18, 19	QA(0:4)	O	LVCMOS	**Clock output bank A**.
22, 23, 26, 27	QB(0:3)	O	LVCMOS	**Clock output bank B**.
30, 31	QC(0,1)	O	LVCMOS	**Clock output bank C**.
8	FB_IN	I, PD	LVCMOS	**Feedback clock input**. Connect to an output for normal operation. This input should be at the same voltage rail as input reference clock. See *Table 1*.
1	VCO_SEL	I, PD	LVCMOS	**VCO divider select input**. See *Table 2*.
5	MR/OE#	I, PD	LVCMOS	**Master reset/output enable/disable input**. See *Table 2*.
9	PLL_EN#	I, PD	LVCMOS	**PLL enable/disable input**. See Table 2.
2, 3, 4	SEL(A:C)	I, PD	LVCMOS	**Frequency select input, Bank (A:C)**. See *Table 2*.
16, 20	V_{DDQA}	Supply	V_{DD}	**2.5V or 3.3V power supply for bank A output clocks**.[2,3]
21, 25	V_{DDQB}	Supply	V_{DD}	**2.5V or 3.3V power supply for bank B output clocks**.[2,3]
32	V_{DDQC}	Supply	V_{DD}	**2.5V or 3.3V power supply for bank C output clocks**.[2,3]
10	AV_{DD}	Supply	V_{DD}	**2.5V or 3.3V power supply for PLL**.[2,3]
11	V_{DD}	Supply	V_{DD}	**2.5V or 3.3V power supply for core and inputs**.[2,3]
7	AV_{SS}	Supply	Ground	**Analog ground**.
13, 17, 24, 28, 29	V_{SS}	Supply	Ground	**Common ground**.

Table 1. Frequency Table

VCO_SEL	Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
0	÷2	Input Clock * 2	100 MHz to 200 MHz	100 MHz to 200 MHz
0	÷4	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
0	÷6	Input Clock * 6	33.33 MHz to 83.33 MHz	33.33 MHz to 66.67 MHz
1	÷2	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 100 MHz
1	÷4	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 50 MHz
1	÷6	Input Clock * 12	16.67 MHz to 41.67 MHz	16.67 MHz to 33.33 MHz

Table 2. Function Table

Control	Default	0	1
VCO_SEL	0	VCO	VCO ÷ 2
PLL_EN#	0	PLL enabled. The VCO output connects to the output dividers	Bypass mode, PLL disabled. The input clock connects to the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO running at its minimum frequency
SELA	0	QA = VCO ÷ 4	QA = VCO ÷ 6
SELB	0	QB = VCO ÷ 4	QB = VCO ÷ 2
SELC	0	QC = VCO ÷ 2	QC = VCO ÷ 4

Notes:
1. PD = Internal pull-down.
2. A 0.1-µF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQA, VDDQB, and VDDQC power supply pins.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		–0.3	5.5	V
V_{DD}	DC Operating Voltage	Functional	2.375	3.465	V
V_{IN}	DC Input Voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{OUT}	DC Output Voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{TT}	Output termination Voltage			$V_{DD} \div 2$	V
LU	Latch Up Immunity	Functional	200		mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Functional		155	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional		42	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional		105	°C/W
ESD_H	ESD Protection (Human Body Model)		2000		Volts
FIT	Failure in Time	Manufacturing test		10	ppm

DC Parameters (V_{DD}= 2.5V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low	LVCMOS			0.7	V
V_{IH}	Input Voltage, High	LVCMOS	1.7		V_{DD} + 0.3	V
V_{OL}	Output Voltage, Low[4]	I_{OL} = 15 mA			0.6	V
V_{OH}	Output Voltage, High[4]	I_{OH} = –15 mA	1.8			V
I_{IL}	Input Current, Low	$V_{IL} = V_{SS}$			–10	µA
I_{IH}	Input Current, High[5]	$V_{IL} = V_{DD}$			100	µA
I_{DDA}	PLL Supply Current	AV_{DD} only		5	10	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins except AV_{DD}		3	5	mA
I_{DD}	Dynamic Supply Current			170		mA
C_{IN}	Input Pin Capacitance			4		pF
Z_{OUT}	Output Impedance			17 – 20		Ω

DC Parameters (V_{DD}= 3.3V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low	LVCMOS			0.8	V
V_{IH}	Input Voltage, High	LVCMOS	2.0		V_{DD} + 0.3	V
V_{OL}	Output Voltage, Low[4]	I_{OL} = 24 mA			0.55	V
		I_{OL} = 12 mA			0.30	
V_{OH}	Output Voltage, High[4]	I_{OH} = –24 mA	2.4			V
I_{IL}	Input Current, Low	$V_{IL} = V_{SS}$			–10	µA
I_{IH}	Input Current, High[5]	$V_{IL} = V_{DD}$			100	µA
I_{DDA}	PLL Supply Current	AV_{DD} only		5	10	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins except AV_{DD}		3	5	mA
I_{DD}	Dynamic Supply Current			240		mA
C_{IN}	Input Pin Capacitance			4		pF
Z_{OUT}	Output Impedance			14 – 17		Ω

Notes:

4. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
5. Inputs have pull-down resistors that affect the input current.

AC Parameters[6] (V_{DD}= 2.5V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{VCO}	VCO Frequency		200		400	MHz
f_{in}	Input Frequency	÷2 Feedback	100		200	MHz
		÷4 Feedback	50		100	
		÷6 Feedback	33.33		66.67	
		÷8 Feedback	25		50	
		÷12 Feedback	16.67		33.33	
		Bypass mode (PLL_EN# = 1)	0		200	
f_{refDC}	Input Duty Cycle		25		75	%
t_r , t_f	TCLK Input Rise/FallTime	0.7V to 1.7V			1.0	ns
f_{MAX}	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		100	
		÷6 Output	33.33		66.67	
		÷8 Output	25		50	
		÷12 Output	16.67		33.33	
DC	Output Duty Cycle	f_{MAX} < 100 MHz	47		53	%
		f_{MAX} > 100 MHz	44		56	
t_r , t_f	Output Rise/Fall times	0.6V to 1.8V	0.1		1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD, does not include jitter	-100		100	ps
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank			125	ps
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at same voltage, same frequency			175	ps
		Banks at same voltage, different frequency			225	
$t_{PLZ, HZ}$	Output Disable Time				8	ns
$t_{PZL, ZH}$	Output Enable Time				10	ns
BW	PLL Closed Loop Bandwidth (-3dB)	÷2 Feedback		2		MHz
		÷4 Feedback		1 - 1.5		
		÷6 Feedback		0.6		
		÷8 Feedback		0.75		
		÷12 Feedback		0.5		
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency			100	ps
		Multiple frequencies			300	
$t_{JIT(PER)}$	Period Jitter	Same frequency			100	ps
		Multiple frequencies			150	
$t_{JIT(\phi)}$	I/O Phase Jitter	VCO < 300 MHz		150		ps
		VCO > 300 MHz		100		
t_{LOCK}	Maximum PLL Lock Time				1	ms

AC Parameters[6] (V_{DD} = 3.3V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{VCO}	VCO Frequency		200		500	MHz
f_{in}	Input Frequency	÷2 Feedback	100		200	MHz
		÷4 Feedback	50		125	
		÷6 Feedback	33.33		83.33	
		÷8 Feedback	25		62.5	
		÷12 Feedback	16.67		41.67	
		Bypass mode (PLL_EN# = 1)	0		200	
f_{refDC}	Input Duty Cycle		25		75	%
t_r , t_f	TCLK Input Rise/FallTime	0.8V to 2.0V			1.0	ns
f_{MAX}	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		125	
		÷6 Output	33.33		83.33	
		÷8 Output	25		62.5	
		÷12 Output	16.67		41.67	
DC	Output Duty Cycle	f_{MAX} < 100 MHz	48		52	%
		f_{MAX} > 100 MHz	44		56	
t_r , t_f	Output Rise/Fall times	0.55V to 2.4V	0.1		1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, same V_{DD}, does not include jitter	–100		200	ps
$t_{sk(O)}$	Output-to-Output Skew	Skew within each Bank			125	ps
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at same voltage, same frequency			175	ps
		Banks at same voltage, different frequency			235	
		Banks at different voltage			425	
$t_{PLZ, HZ}$	Output Disable Time				8	ns
$t_{PZL, ZH}$	Output Enable Time				10	ns
BW	PLL Closed Loop Bandwidth (-3dB)	÷2 Feedback		2		MHz
		÷4 Feedback		1 – 1.5		
		÷6 Feedback		0.6		
		÷8 Feedback		0.75		
		÷12 Feedback		0.5		
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency			100	ps
		Multiple frequencies			275	
$t_{JIT(PER)}$	Period Jitter	Same frequency			100	ps
		Multiple frequencies			150	
$t_{JIT(\phi)}$	I/O Phase Jitter	VCO < 300 MHz		150		ps
		VCO > 300 MHz		100		
t_{LOCK}	Maximum PLL Lock Time				1	ms

Note:

6. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at the same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

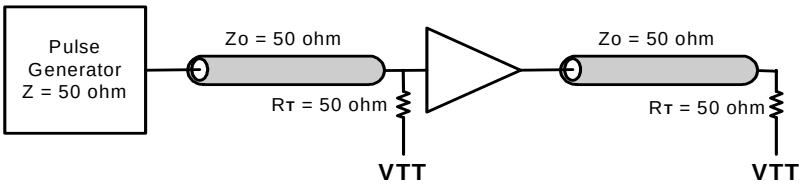


Figure 1. AC Test Reference for V_{DD} = 3.3V / 2.5V

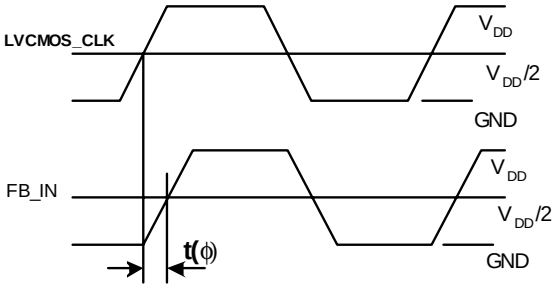


Figure 2. Propagation Delay t(ϕ), static phase offset

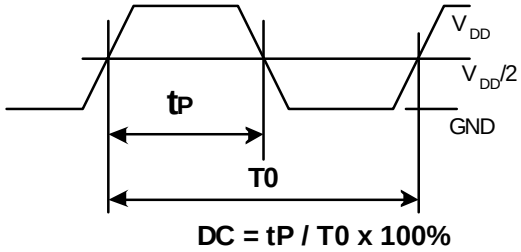


Figure 3. Output Duty Cycle (DC)

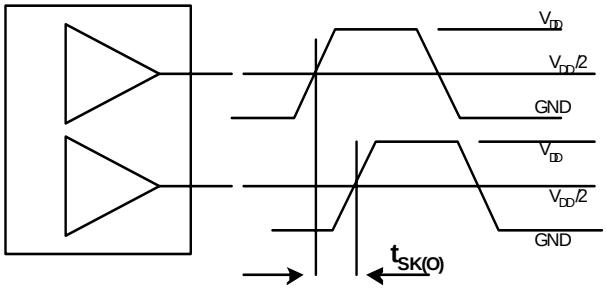


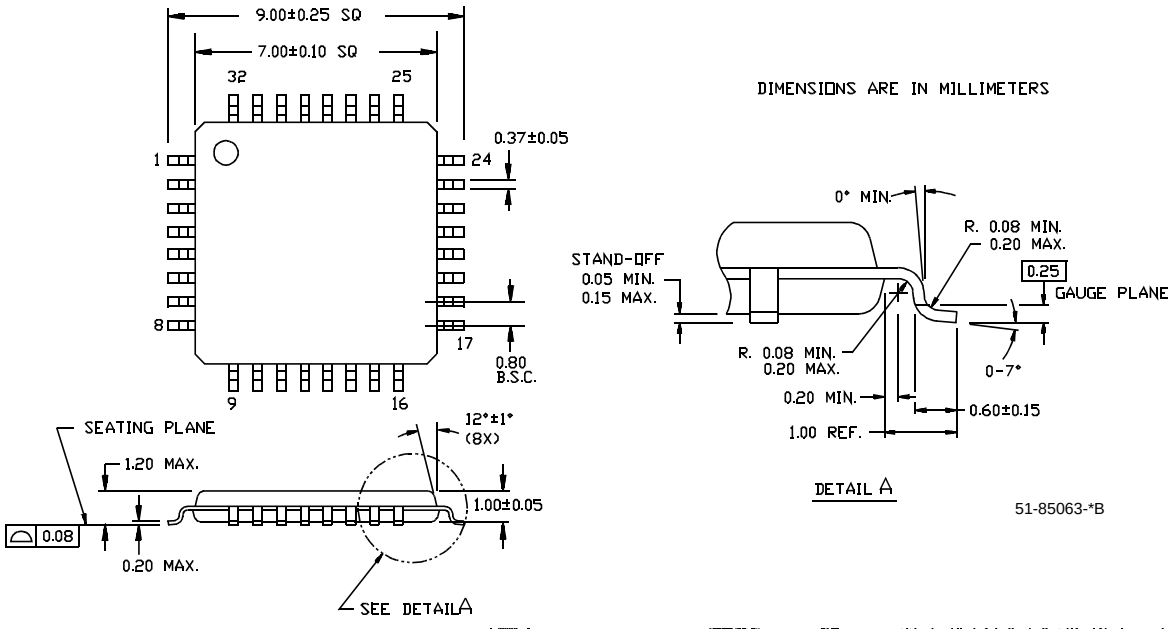
Figure 4. Output-to-Output Skew, $t_{sk(O)}$

Ordering Information

Part Number	Package Type	Product Flow
CY29352AI	32-pin TQFP	Industrial, –40°C to +85°C
CY29352AIT	32-pin TQFP – Tape and Reel	Industrial, –40°C to 85°C

Package Drawing and Dimension

32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm A32



Document History Page

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REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	124654	03/21/03	RGL	New Data Sheet