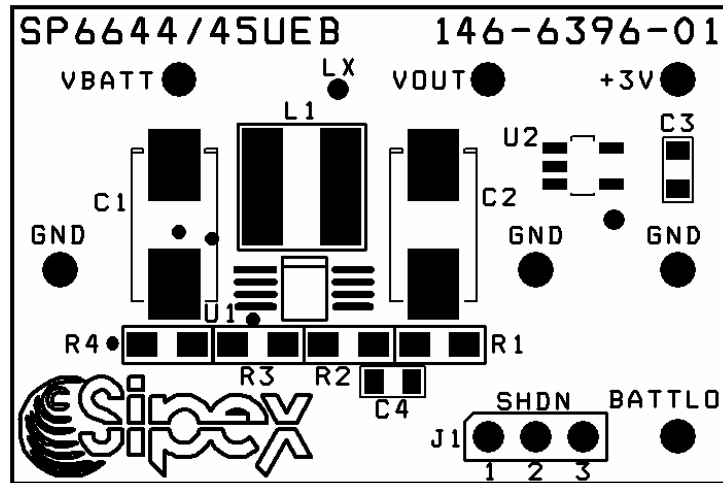




SP6644/6645 Evaluation Board Manual

- Easy Evaluation for the SP6644/6645 Single or Dual Cell Alkaline to 3.3V Output
- Provides up to 150mA output current for 2-Cell Input
- High Efficiency: 92%
- μ SOIC Package & SMT components for small, low profile Power Supply



DESCRIPTION

The **SP6644/6645 Evaluation Board** is designed to help the user evaluate the performance of the SP6644/6645 for use as a single or dual cell input to +3.3V output DC-DC Converter. The output of the SP6644/6645 is preset to +3.3V or can be adjusted from +2V to +5.5V by manipulating two external resistors. The SP6644/6645UEB evaluation board is a complete power supply circuit with an option for adding a small SOT23 5-pin +3V LDO Regulator to provide even better regulation and low noise output.

The evaluation board is a completely assembled and tested surface mount board which provides easy probe access points to all SP6644/6645 Inputs and Outputs so that the user can quickly connect and measure electrical characteristics and waveforms.

The next two sections describe the SP6644/6645 Board Layout and Using the SP6644/6645 Evaluation Boards. Power Supply Data is supplied as measured from a typical SP6644/6645 evaluation board. The SP6644/6645 Evaluation Board List of Materials table is provided with some manufacturers part numbers to use as a reference. Finally, a schematic and drawings of the PC Layout are included as a design-in tool for the user of the SP6644/6645.

BOARD LAYOUT

The **SP6644/6645 Evaluation Board** has been designed for easy and convenient access to all Inputs and Outputs of the SP6644/6645 device under test. Position the board with the silkscreen lettering upright, (also see the drawing on the front page of this manual) and you will see U1 the SP6644/6645 8-pin μ SOIC, in the center left of the board. To the left of U1 are the input capacitor C1 and the Vbatt pin. To the right of U1 are the output capacitor C2 and the Vout post. Above U1 is the inductor L1 and the LX test point.

USING THE EVALUATION BOARD

1) Powering Up the SP6644/6645 Circuit

The SP6644/6645 Evaluation Board can be powered from inputs from a +0.8V to +3.3V from 1 or 2 alkaline cells or a power supply. Connect with short leads directly to the “Vbatt” and “Gnd” posts. Monitor the Output Voltage and connect the Load between the “Vout” post and the 2nd “GND” post.

2) Using the J1 Jumper: Enabling the SP6644/6645 Output and using the Shutdown Mode

The SP6644/6645 output will be Enabled if the J1 Jumper is in the left or pin 1 to 2 position. If J1 is in the pin 2 to 3 position, the Shutdown pin is brought to GND, which puts the SP6644/6645 in the low quiescent Shutdown Mode.

3) Using the LDO Output

The SP6644/6645 output connects to an LDO, the SP6201 ultra low drop-out CMOS regulator which has a 3.0V output at up to 150mA. To evaluate the SP6201 performance with the SP6644/6645 input, connect the load across the +3V post and GND and measure both the SP6644/6645 output and SP6201 output with an oscilloscope configured for AC millivolts. As you can see from figure 8 the output ripple voltage is reduced from 60mV to less than 3mV by the LDO.

4) Using the Rlim Function

The peak inductor current, I_{PEAK} , is programmed externally by the RLIM resistor connected between the RLIM pin and GND. The peak inductor current is defined by:

$$I_{PEAK} = 1400/R_{LIM}$$

The SP6644/45 datasheet specifications for RLIM give a range of 2.5 to 9.3K ohms. Using the IPEAK equation above gives an IPEAK range of

$$I_{PEAK} \text{ range} = 150 \text{ to } 560\text{mA.}$$

The saturation current specified for the inductor needs to be greater then the peak current to avoid saturating the inductor, which would result in a loss in efficiency and could damage the inductor. The SP6644/6645 evaluation board uses a Rlim value of 2.5K to allow the circuit to deliver up to 80mA for 1.3V input and 150mA for 2.6V input. Other values could be selected using the above relationships.

POWER SUPPLY DATA

The SP6644/6645's high efficiency is illustrated in figures 1 & 2 which has 90 to 93% efficiency for 2 fully charged alkaline cells. Figure 1 with Rlim of 2.5K can deliver more output current than figure 2 with an Rlim of 5K because it has greater peak current, at a price of reduced efficiency. Line/Load curves in figures 3 & 4 show only 10 to 15mV change in output voltage at rated loads of 80mA for 1-cell and 150mA for 2-cell. The no-load battery current the SP6644/6645 application circuit consumes for different Rlim's of 2.5K & 5K is illustrated in figure 5. In figure 6 the maximum load current the SP6644/6645 can deliver for different Rlim's of 2.5K & 5K is illustrated. Load transient response to a 15mA to 150mA output load step is shown in figure 7. Finally, in figure 8, SP6644 output ripple of 60mV is improved with the addition of the SP6201 LDO achieving an output ripple of only 3mV.

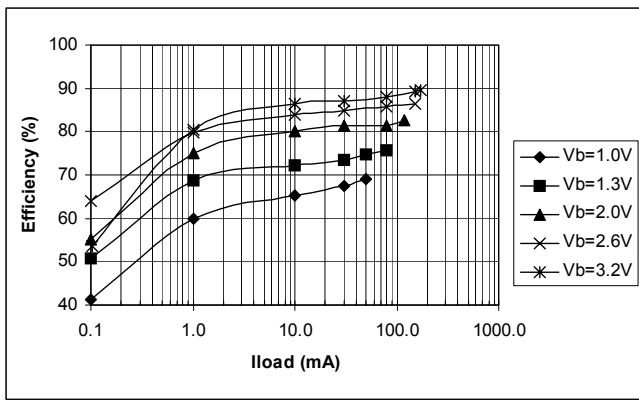


Figure 1. Efficiency Vs Output Current (Vout = 3.3V) Rlim=2.5K

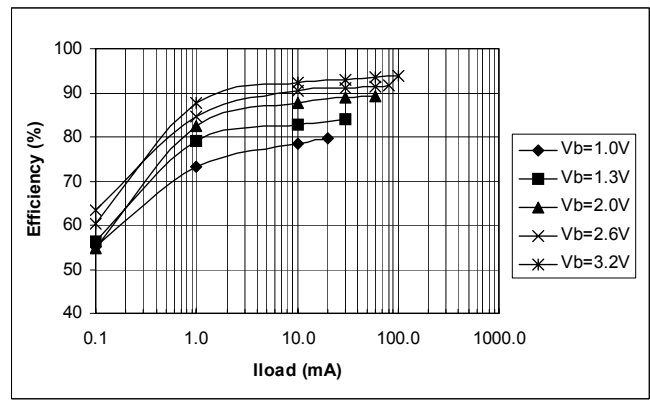


Figure 2. Efficiency Vs Output Current (Vout = 3.3V) Rlim=5K

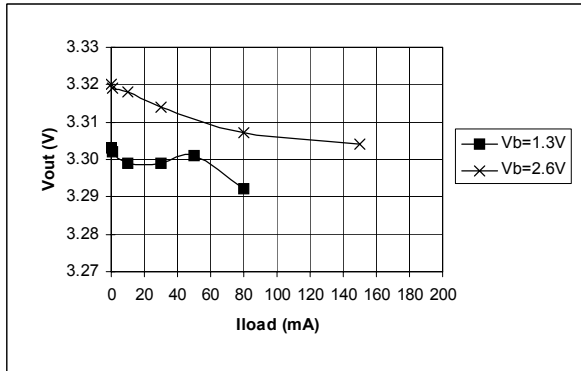


Figure 3. Line/Load Rejection Vs Output Current (Vout = 3.3V) Rlim=2.5K

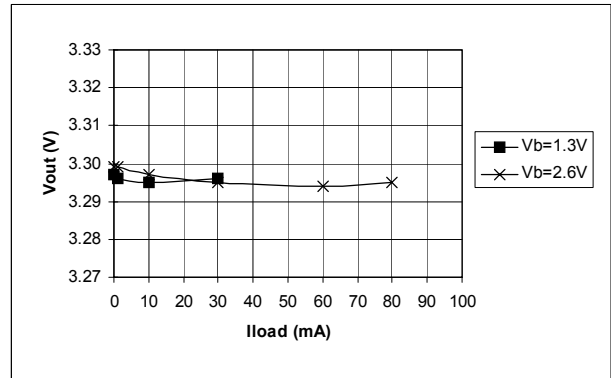


Figure 4. Line/Load Rejection Vs Output Current (Vout = 3.3V) Rlim=5K

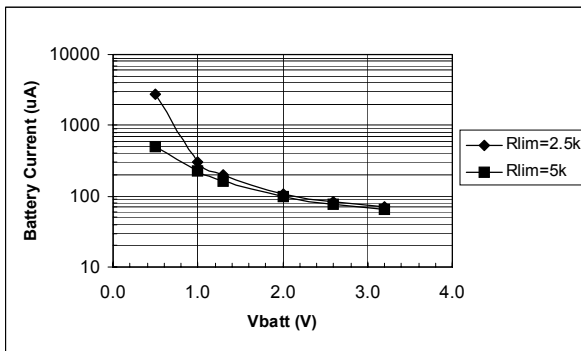


Figure 5. No-Load Battery Current Vs Vbatt (Vout = 3.3V)

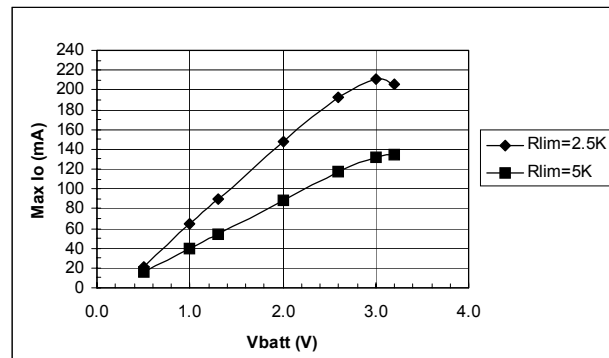


Figure 6. Maximum Load Current Vs Vbatt (Vout = 3.3V)

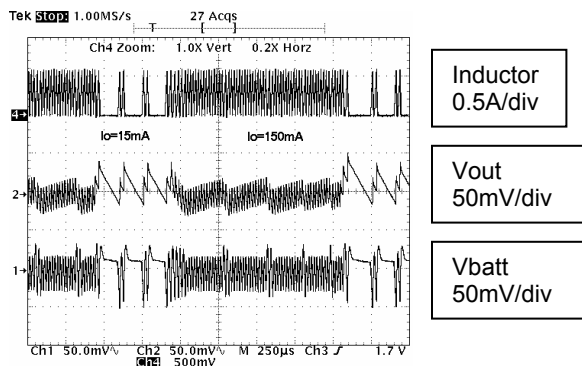


Figure 7. Load Transient Response Rlim=2.5K (Vin = 1.3V, Vout = 3.3V)

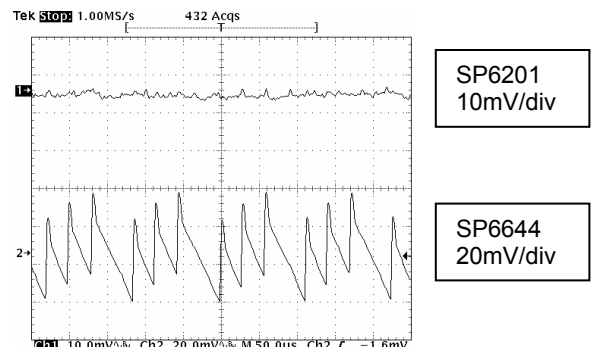


Figure 8. SP6644 and SP6201 Output Ripple Rlim=2.5K (Vin = 1.3V, Vout = 3.3V, Iout=80mA)

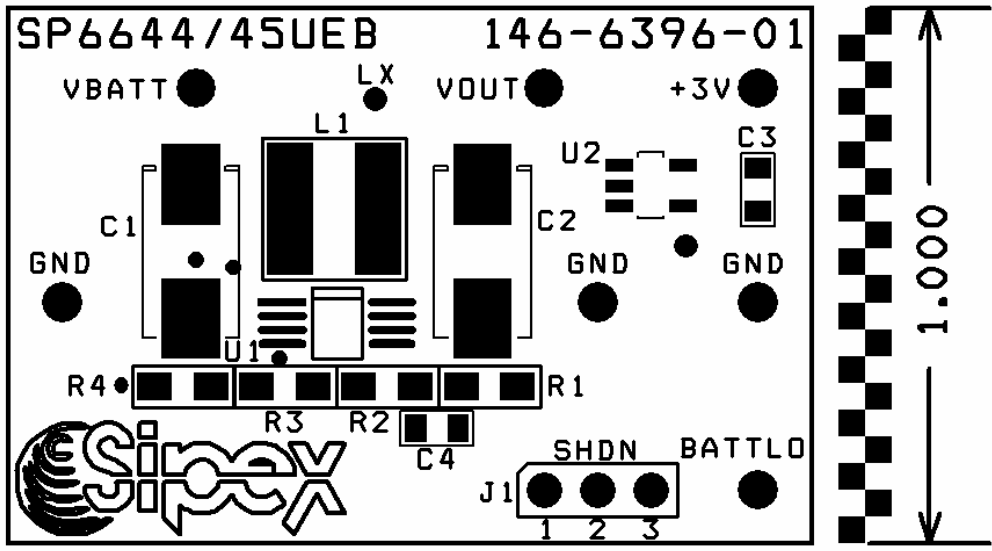


FIGURE 9: SP6644/6645UEB COMPONENT PLACEMENT

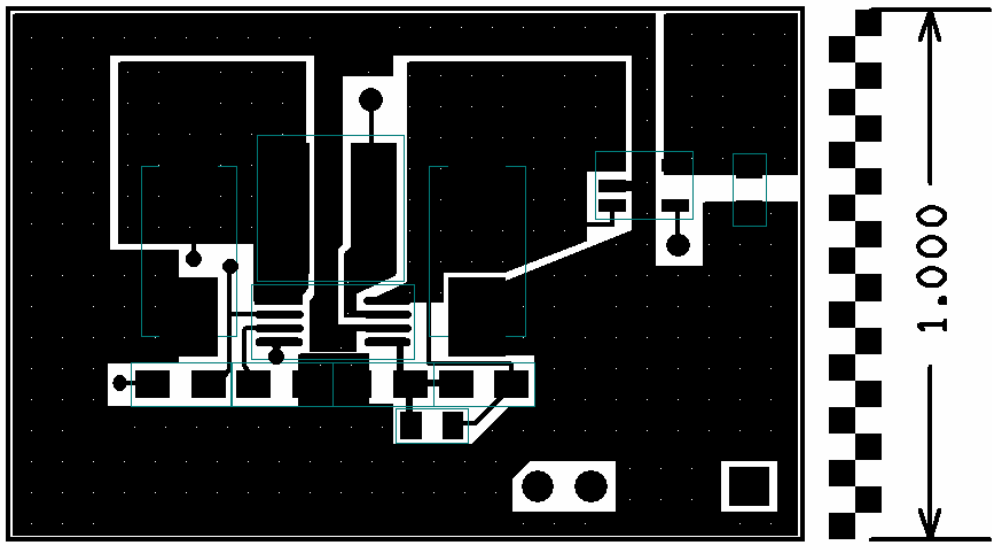


FIGURE 10: SP6644/6645UEB PC LAYOUT TOP SIDE

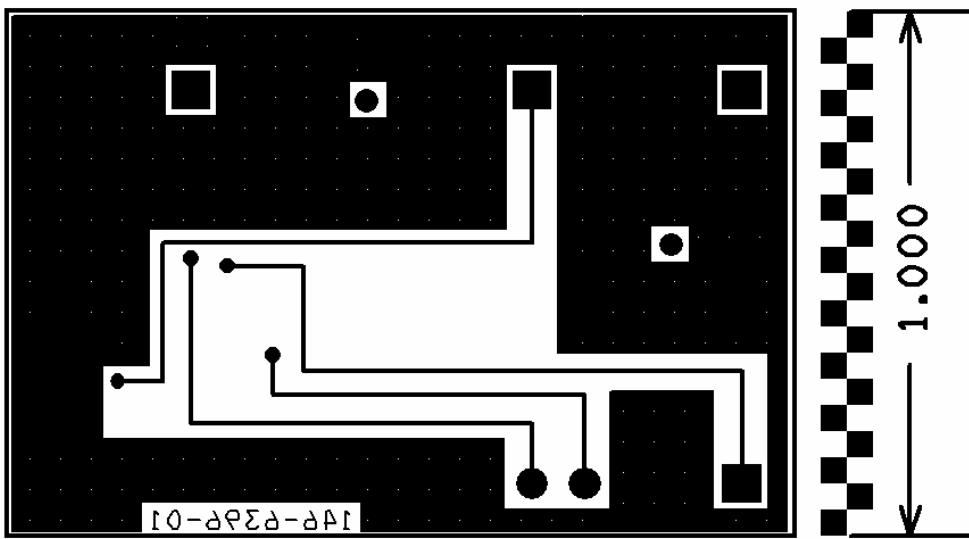


FIGURE 11: SP6644/6645UEB PC LAYOUT BOTTOM SIDE

